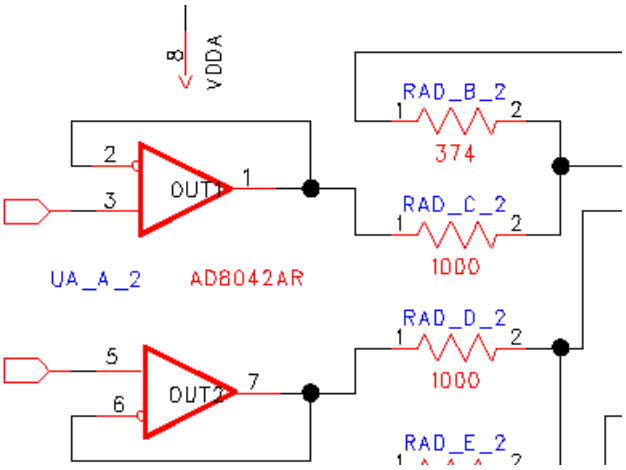
ATLAS LAr FEB Schematics



Submitted for review 2001-SEP-20.

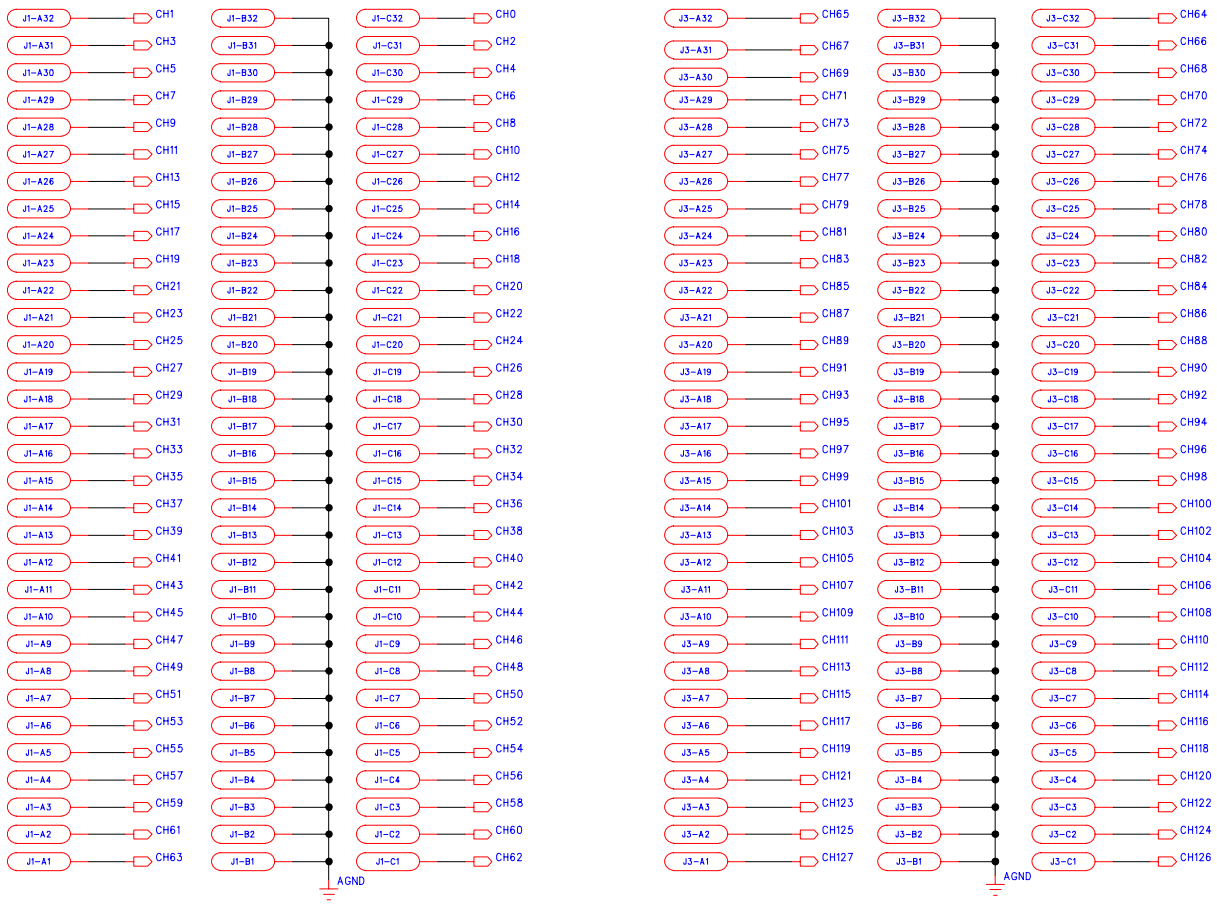
- Input Signal Connectors: PS, PS.gz, png, PNG, Tiff.
- Top Slice: PS, PS.gz, png, PNG, Tiff.
- Bottom Slice: PS, PS.gz, png, PNG, Tiff.
- Trigger Sums: PS, PS.gz, png, PNG, Tiff.
- ADCs: PS, PS.gz, png, PNG, Tiff.
- Gain Selector 0-1: PS, PS.gz, png, PNG, Tiff.
- Gain Selector 2-3: PS, PS.gz, png, PNG, Tiff.
- Gain Selector 4-5: PS, PS.gz, png, PNG, Tiff.
- Gain Selector 6-7: PS, PS.gz, png, PNG, Tiff.
- Front-End-Link with SMUX: PS.
- Front-End-Link with DMUX (OBSOLETE): PS, PS.gz, png, PNG, Tiff.
- SCA Controller: PS, PS.gz, png, PNG, Tiff.
- SCA control bus: PS, PS.gz, png, PNG, Tiff.
- TTCrx: PS, PS.gz, png, PNG, Tiff.
- Clock Fanout: PS, PS.gz, png, PNG, Tiff.
- SPAC Configuration Controller: PS, PS.gz, png, PNG, Tiff.
- Power Connector: PS, PS.gz, png, PNG, Tiff.
- Front End Regulators: PS, PS.gz, png, PNG, Tiff.
- Back End Regulators: PS, PS.gz, png, PNG, Tiff.
- Voltage/Temperature Monitoring: PS
- Testpoints: PS, PS.gz, png, PNG, Tiff.
- Mounting Holes: PS, PS.gz, png, PNG, Tiff.

- Layout Front
- Layout Back
- Stackup .

Last modified: Thu Sep 20 21:35:54 EDT 2001

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Input signal connectors



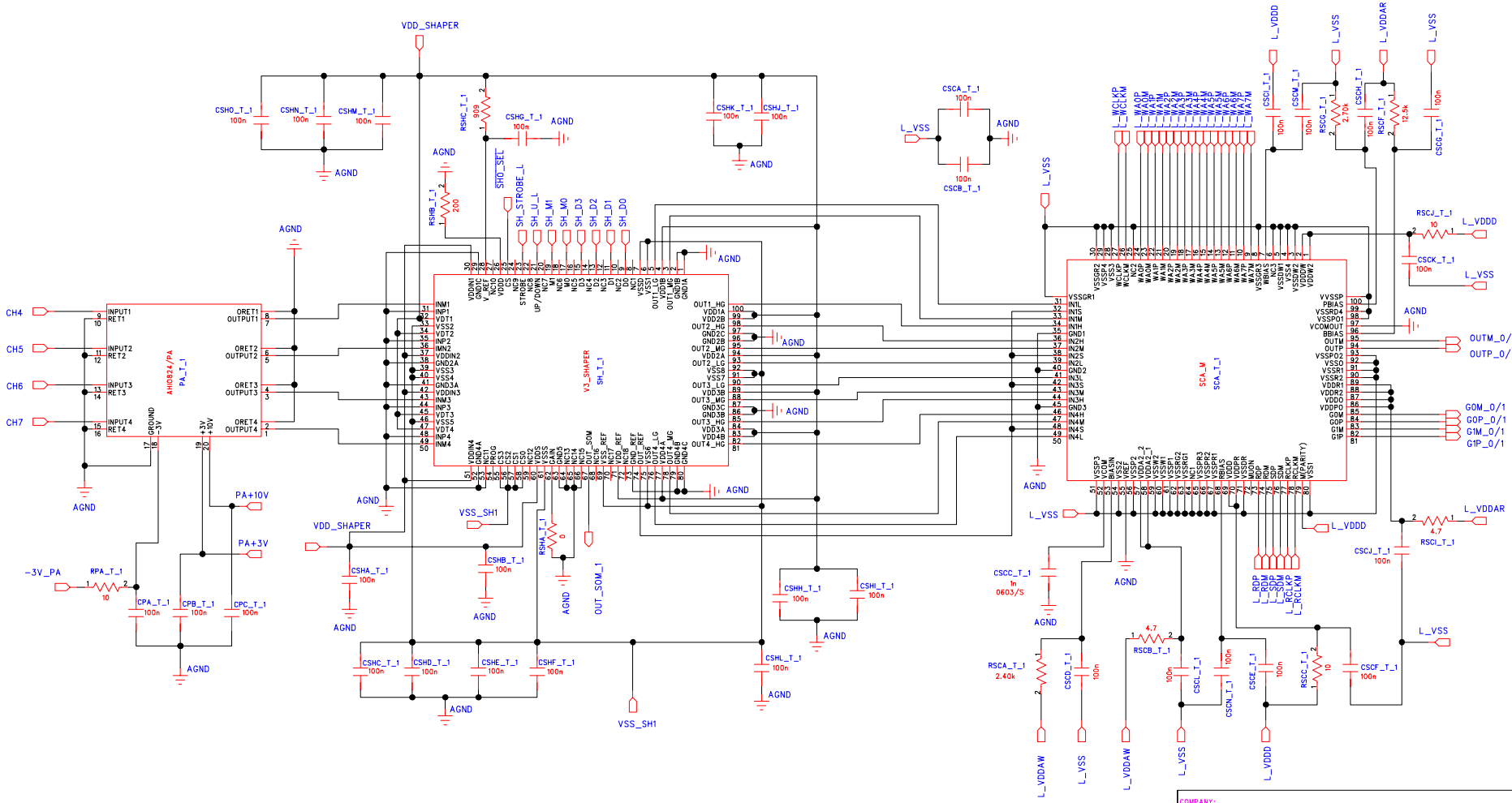
Channels 0–3 are connected to the "bottom" PA
Channel 0 is connected to the PA pin #15

Channels 4–7 are connected to the "top" PA
Channel 4 is connected to the PA pin #9

DRAWN:	DATED:	COMPANY: NEVIS-LABS COLUMBIA UNIVERSITY		
CHECKED:	DATED:	TITLE: FEB-INPUT SIGNAL CONNECTORS		
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO: / REV:
RELEASED: jb	DATED: august/01	SCALE:		SHEET: 7 OF

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

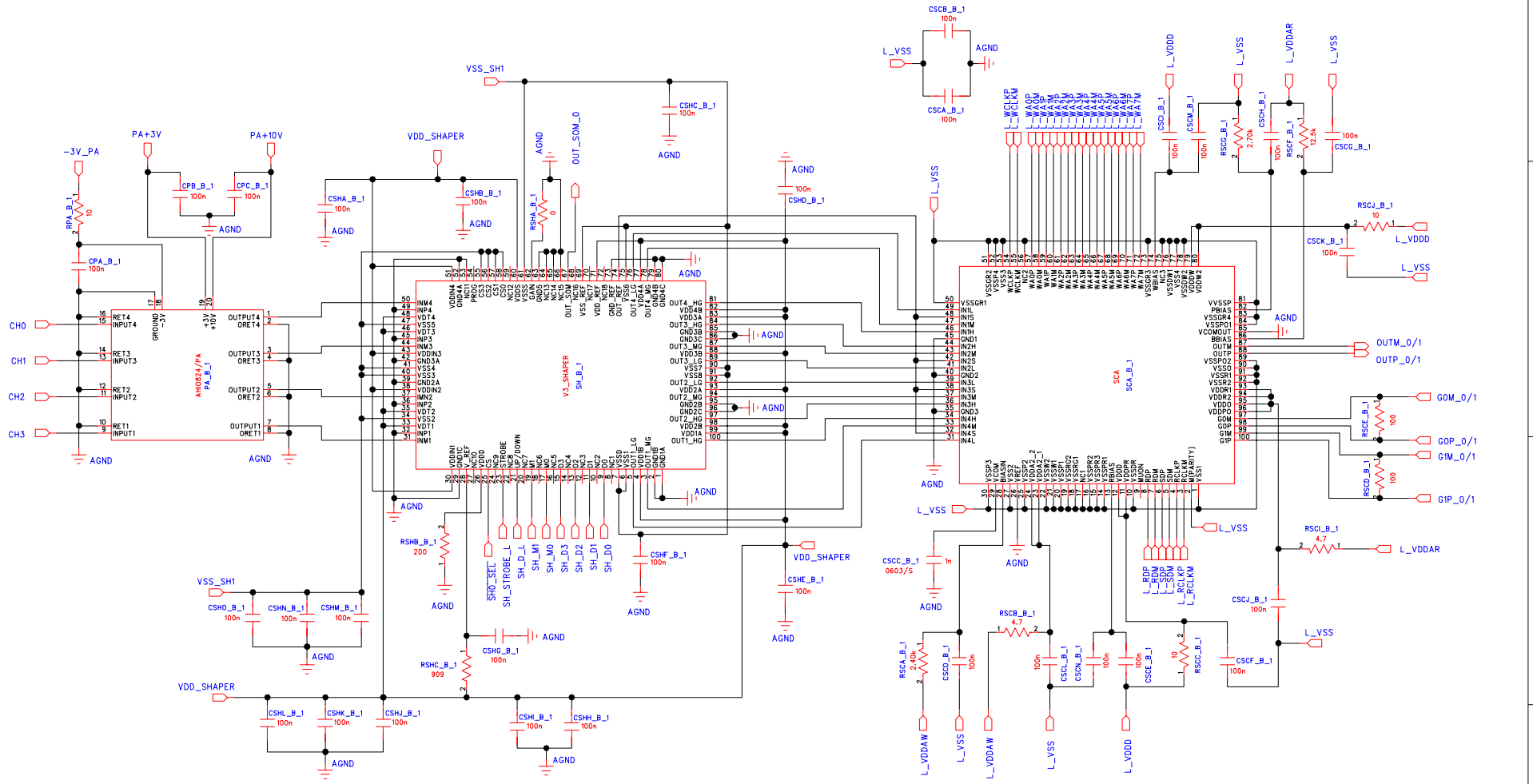
Top side slice



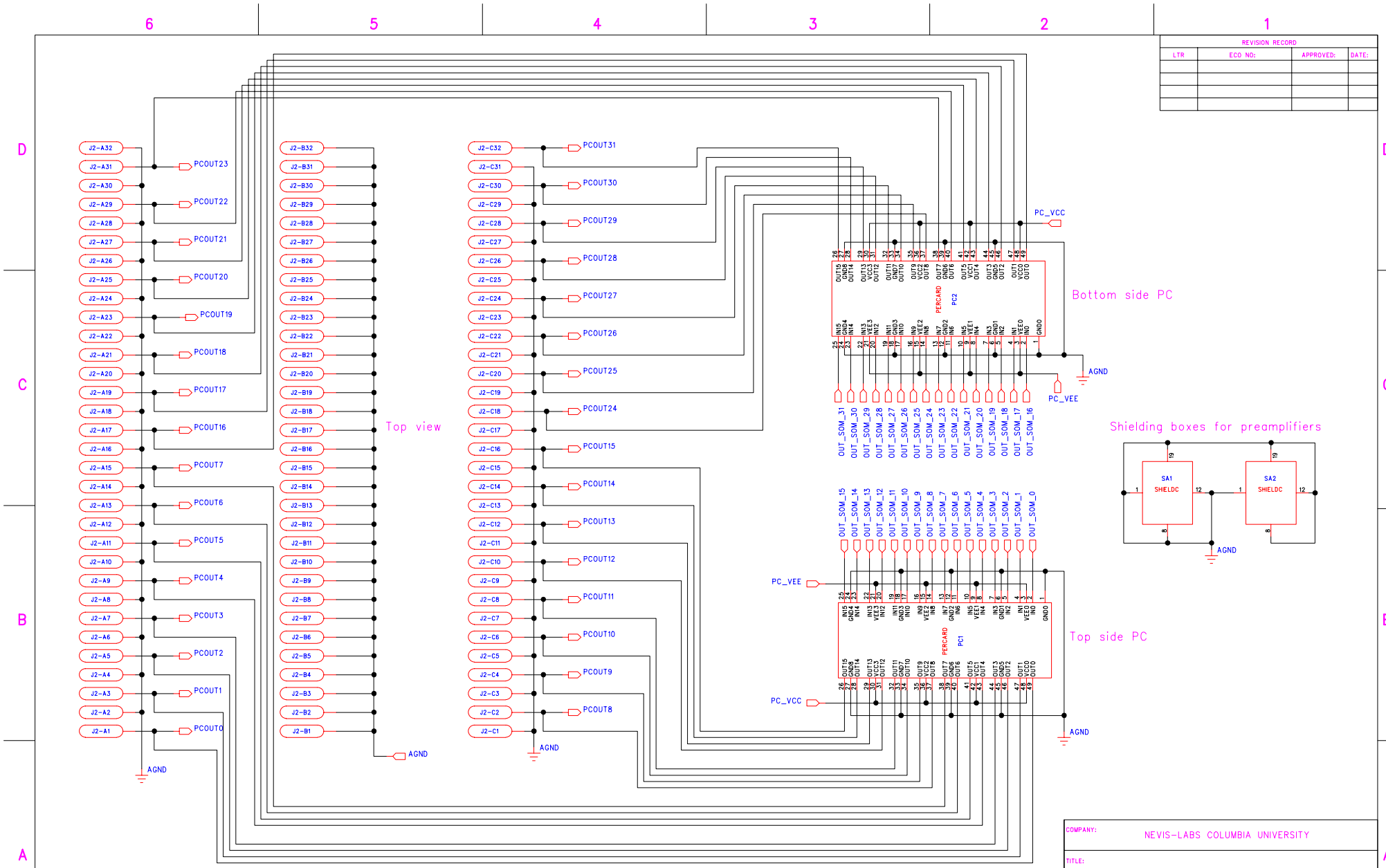
DRAWN:	DATED:	COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: Atlas FEB SLICE#1 SCHEMATICS	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO:	REV:
RELEASED: jb	DATED: march/01	SCALE:	SHEET: 9 OF

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Bottom side slice

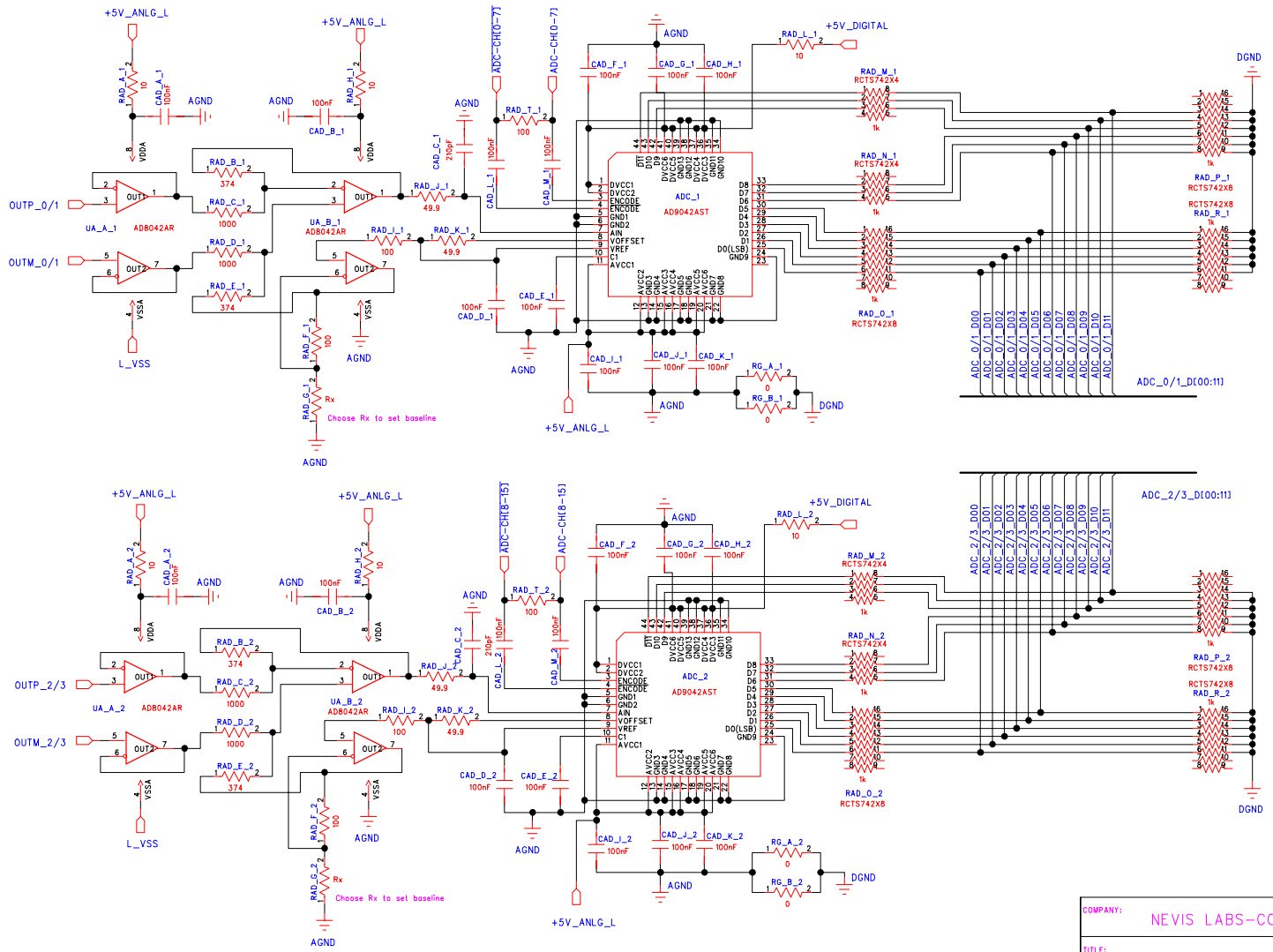


DRAWN:	DATED:	COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: Atlas FEB SLICE#0 SCHEMATICS	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO:	REV:
RELEASED: jb	DATED: march/01	SCALE:	SHEET: 8 OF



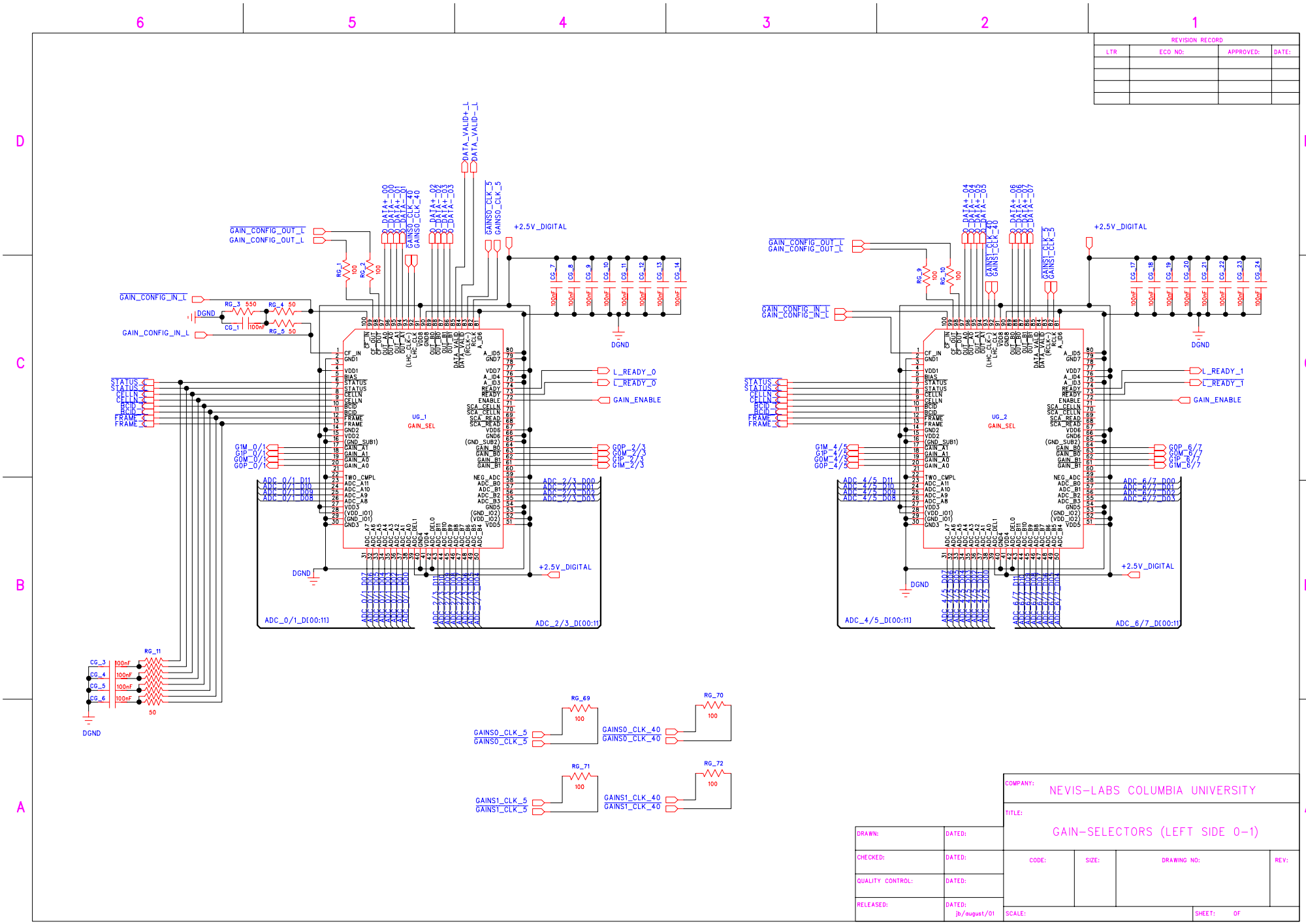
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY:	NEVIS-LABS COLUMBIA UNIVERSITY		
TITLE:	ATLAS FEB TRIGGER SIGNALS		
DRAWN:	DATED:	CODE:	SIZE:
CHECKED:	DATED:	DRAWING NO:	REV:
QUALITY CONTROL:	DATED:		
RELEASED: jb	DATED: sept./98	SCALE:	SHEET: 6 OF

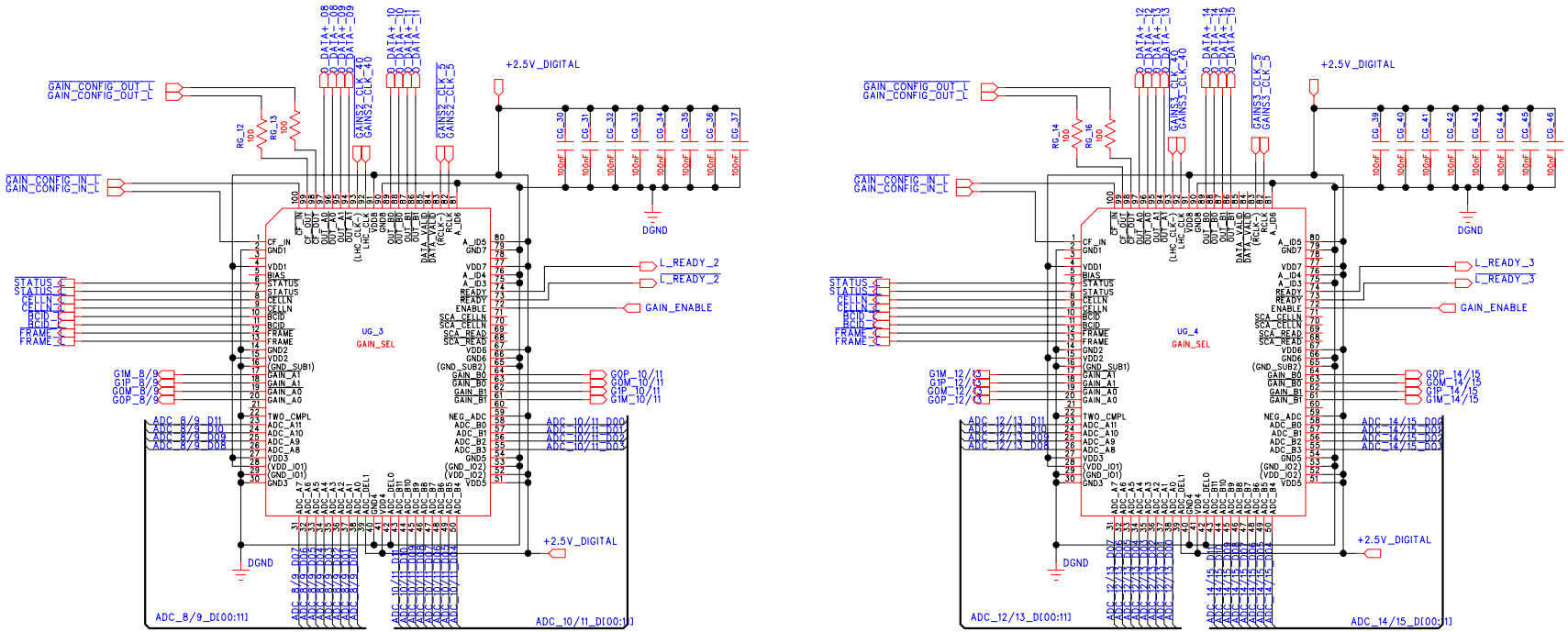


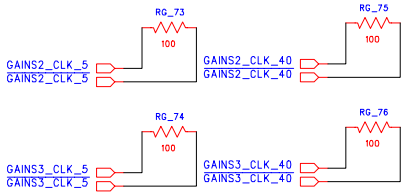
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY			
TITLE: Atlas FEB – ADC Channels 0-15			
DRAWN:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	DATED:				
QUALITY CONTROL:	DATED:				
RELEASED: jb	DATED: april/01	SCALE:		SHEET: OF	


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
GAIN_CONFIG_OUT_L
GAIN_CONFIG_IN_L
+2.5V_DIGITAL
DGND
UG_1
GAIN_SEL
UG_2
GAIN_SEL
L_READY_0
L_READY_1
GAIN_ENABLE
ADC_0/1_D[00:11]
ADC_2/3_D[00:11]
ADC_4/5_D[00:11]
ADC_6/7_D[00:11]
RG_69
RG_70
RG_71
RG_72
COMPANY:
NEVIS-LABS COLUMBIA UNIVERSITY
TITLE:
GAIN-SELECTORS (LEFT SIDE 0-1)
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb/august/01
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET:
OF

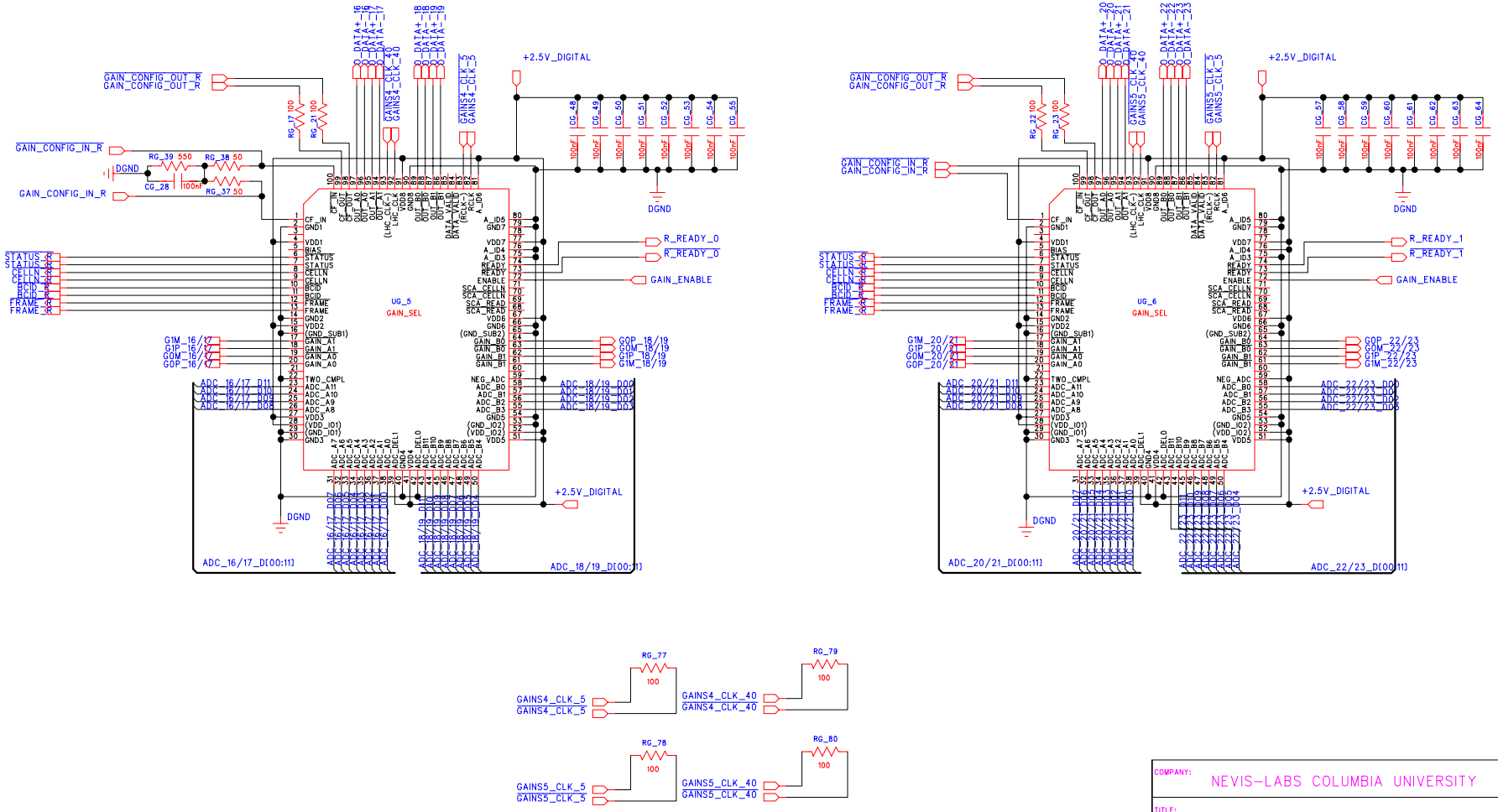
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



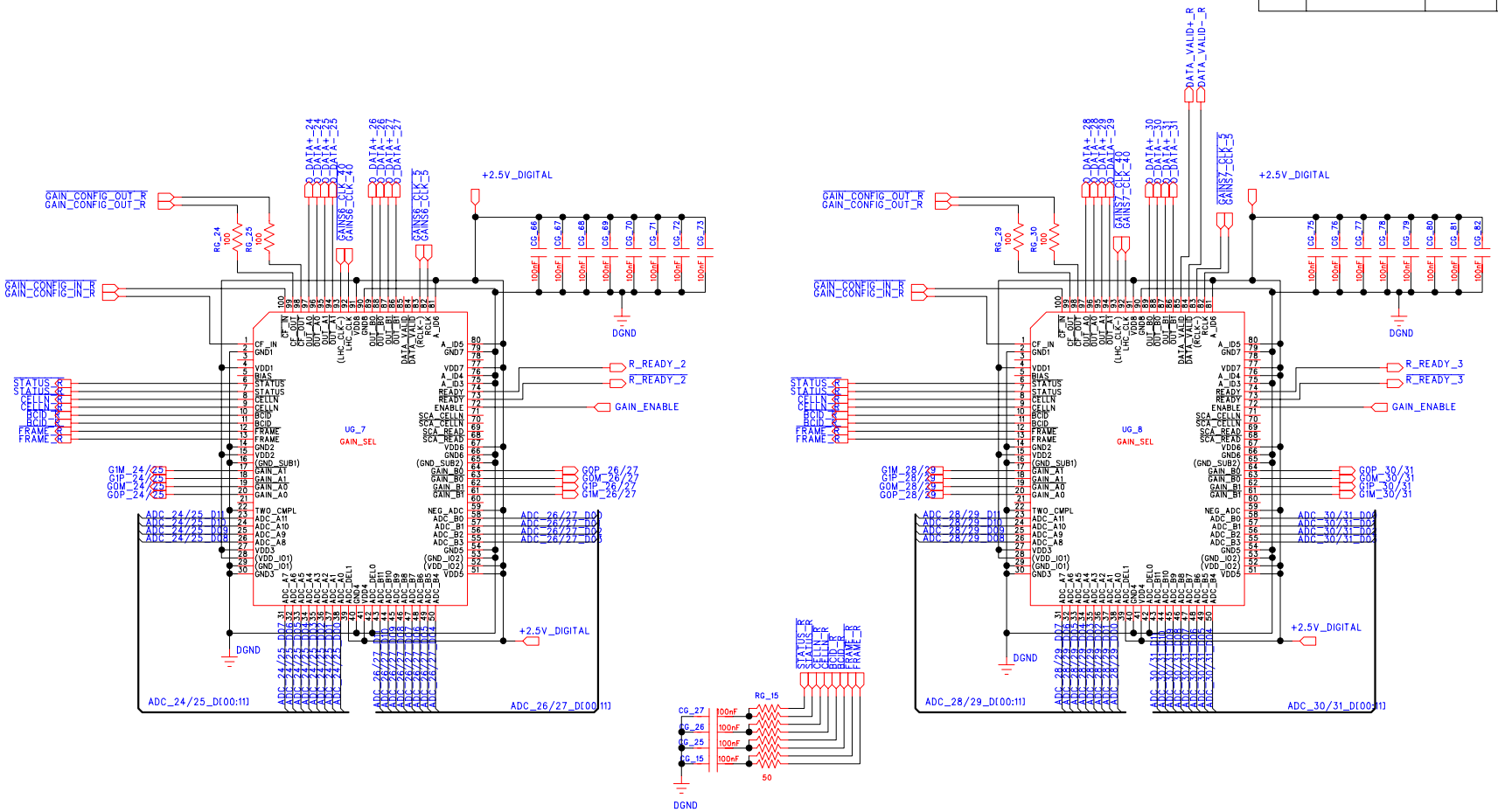


DRAWN:	DATED:	COMPANY: NEVIS-LABS COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: GAIN-SELECTORS (LEFT SIDE 2-3)	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO:	REV:
RELEASED:	DATED: jb/may/01	SCALE:	SHEET: OF

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

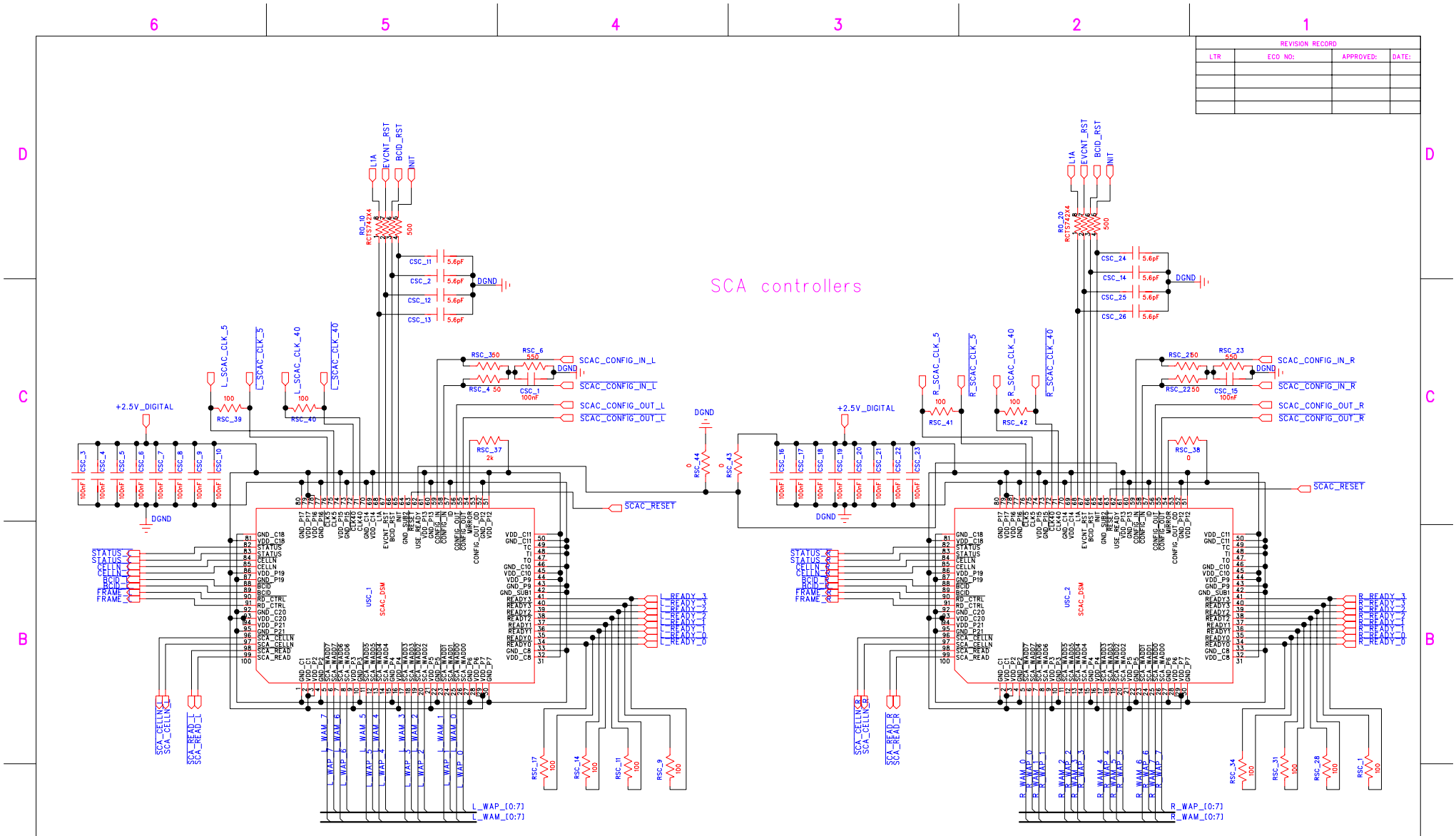


DRAWN:	DATED:	COMPANY: NEVIS-LABS COLUMBIA UNIVERSITY		
CHECKED:	DATED:	TITLE: GAIN-SELECTORS (RIGHT SIDE 4-5)		
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO: / REV:
RELEASED:	DATED: jb/may/01	SCALE:		SHEET: OF



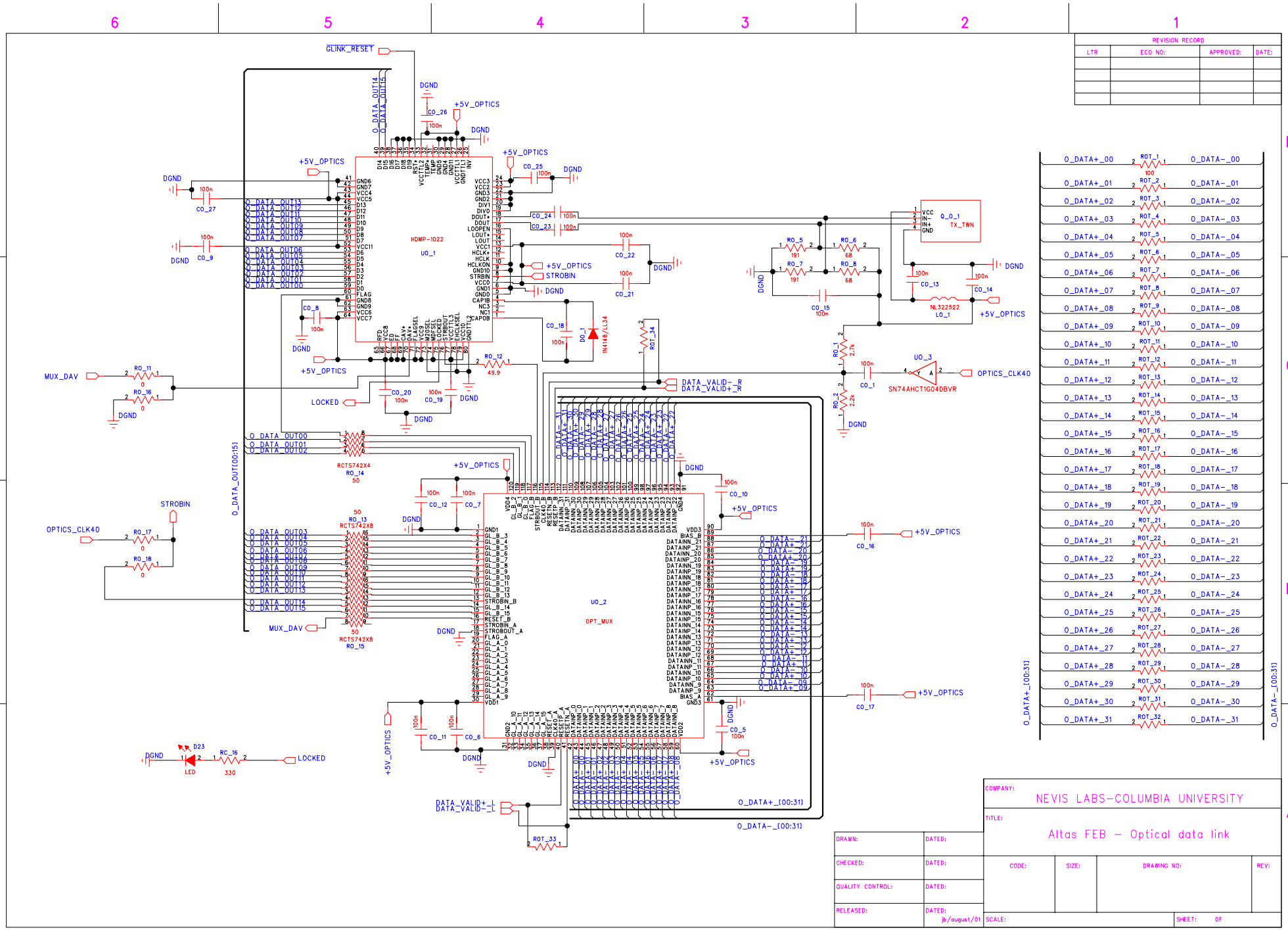
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

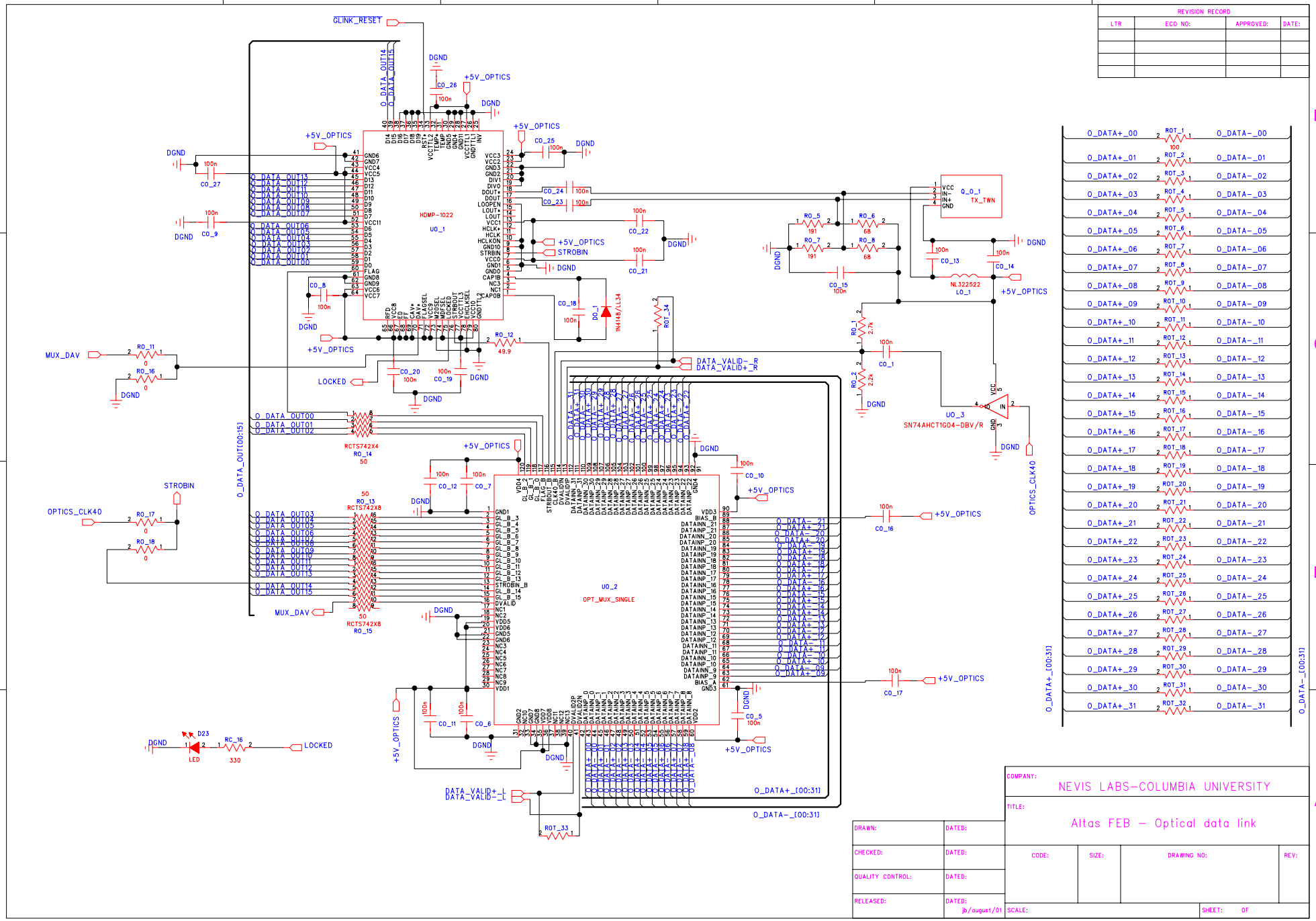
COMPANY: NEVIS-LABS COLUMBIA UNIVERSITY			
TITLE: GAIN-SELECTORS (RIGHT SIDE (6-7)			
DRAWN:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	DATED:				
QUALITY CONTROL:	DATED:				
RELEASED:	DATED: jb/may/01	SCALE:		SHEET: OF	

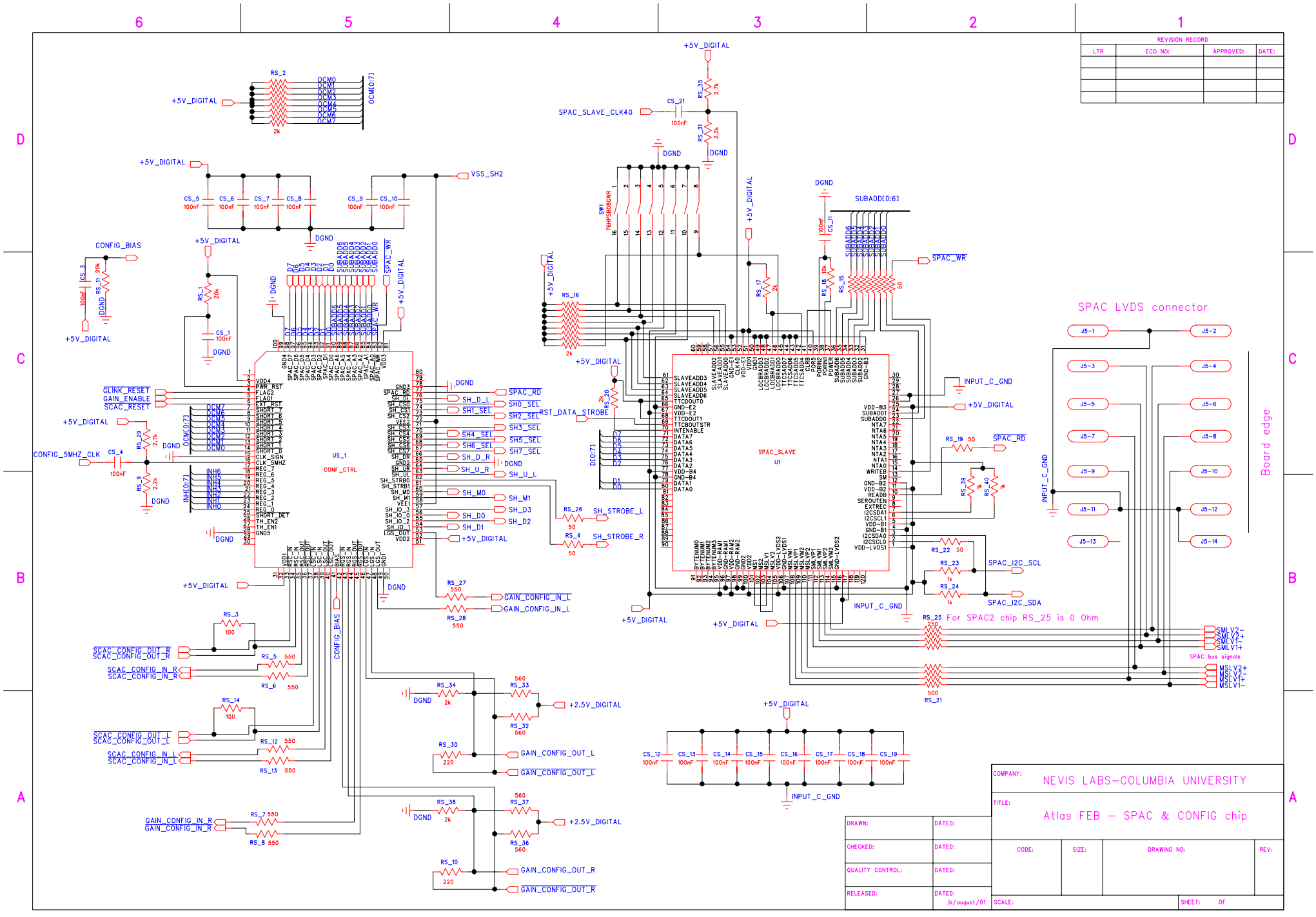


REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

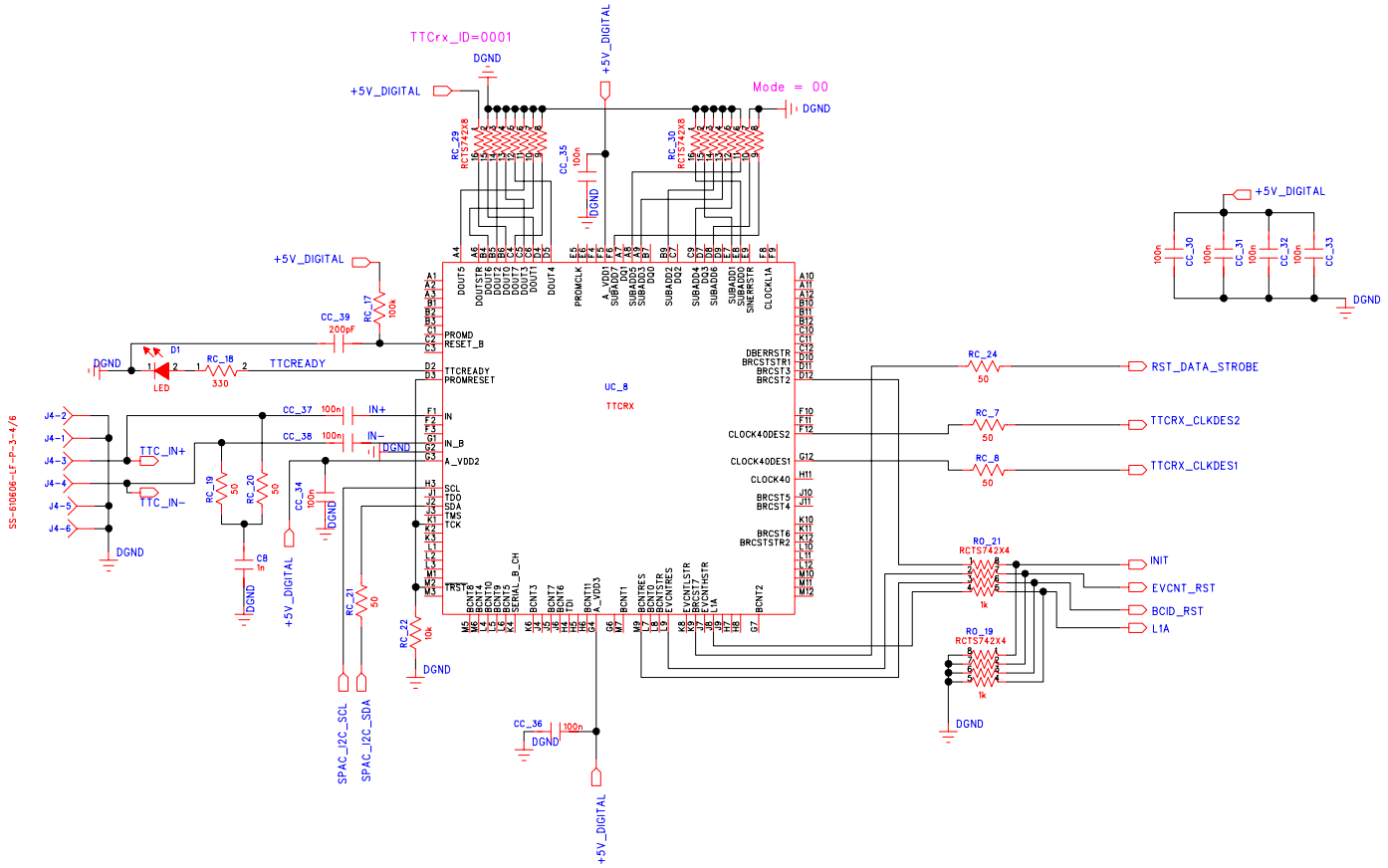
DRAWN:	DATED:	COMPANY: NEVIS-LABS COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: ATLAS FEB – SCAC chips	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO:	REV:
RELEASED:	DATED: jb/may/01	SCALE:	SHEET: OF


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
GLINK_RESET
HDMP-1022
U0_1
Q_0_1
TX_TWN
NL322522
L0_1
SN74AHCT1G04DBVR
OPTICS_CLK40
MUX_DAV
STROBIN
LOCKED
DATA_VALID-_R
DATA_VALID+_R
DATA_VALID+_L
DATA_VALID-_L
O_DATA_OUT[00:15]
O_DATA+_[00:31]
O_DATA-_[00:31]
U0_2
OPT_MUX
RCTS742X4
RCTS742X8
+5V_OPTICS
DGND
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
Altas FEB - Optical data link
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb/august/01
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET:
OF

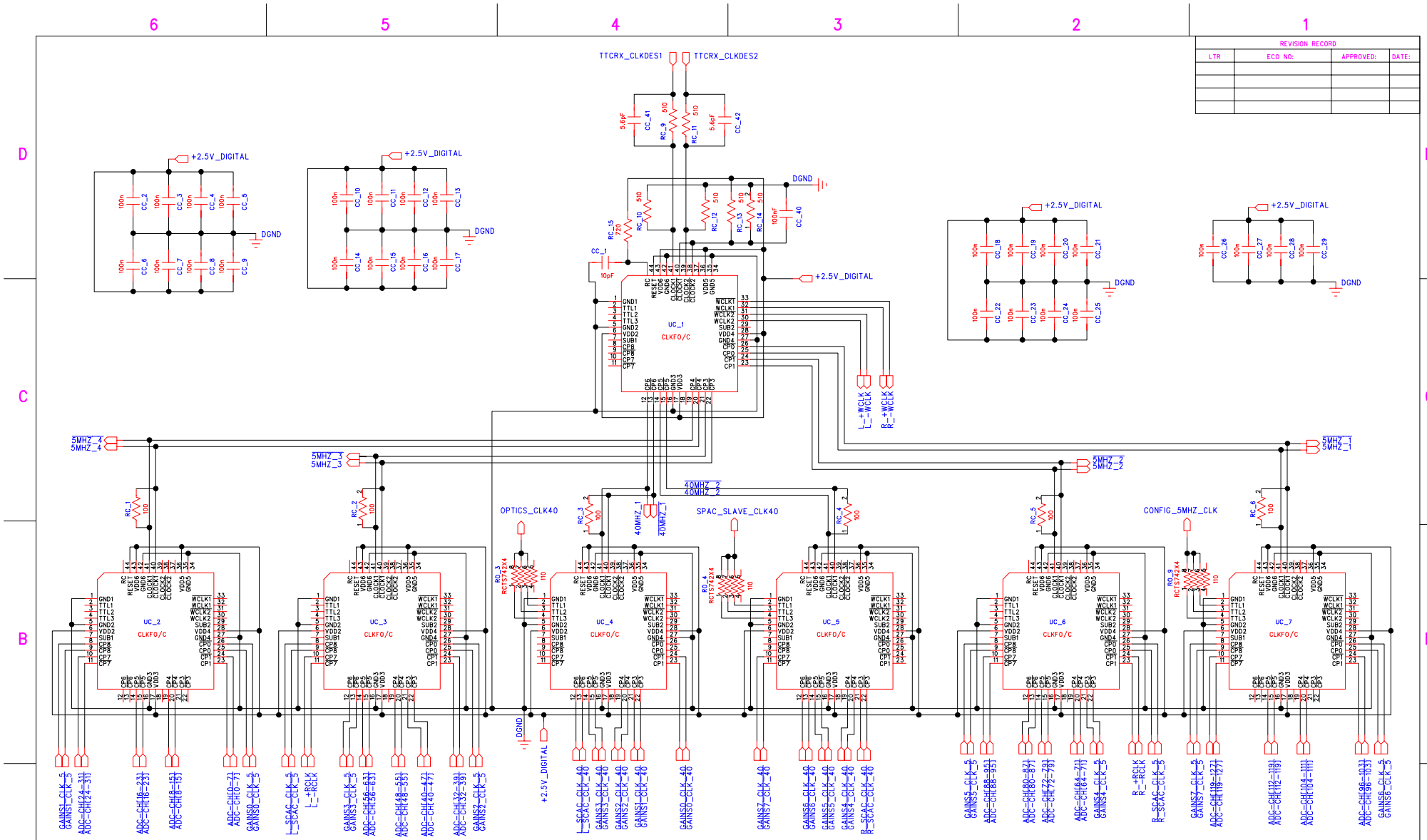

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
GLINK_RESET
HDMP-1022
U0_1
Q_0_1
TX_TWN
NL322522
L0_1
SN74AHCT1G04-DBV/R
U0_3
OPT_MUX_SINGLE
U0_2
RCTS742X4
RO_14
RCTS742X8
RO_13
RO_15
MUX_DAV
OPTICS_CLK40
STROBIN
LOCKED
DATA_VALID-_R
DATA_VALID+_R
DATA_VALID+_L
DATA_VALID-_L
O_DATA_OUT[00:15]
O_DATA+_[00:31]
O_DATA-_[00:31]
+5V_OPTICS
DGND
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
Altas FEB - Optical data link
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb/august/01
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET:
OF


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
SPAC LVDS connector
Board edge
SPAC_SLAVE
U1
US_1
CONF_CTRL
SPAC_SLAVE_CLK40
RST_DATA_STROBE
SUBADD[0:6]
SPAC_WR
SPAC_RD
SPAC_I2C_SCL
SPAC_I2C_SDA
INPUT_C_GND
+5V_DIGITAL
DGND
VSS_SH2
CONFIG_BIAS
CONFIG_5MHZ_CLK
GLINK_RESET
GAIN_ENABLE
SCAC_RESET
SH_STROBE_L
SH_STROBE_R
GAIN_CONFIG_IN_L
GAIN_CONFIG_IN_R
GAIN_CONFIG_OUT_L
GAIN_CONFIG_OUT_R
SCAC_CONFIG_OUT_R
SCAC_CONFIG_IN_R
SCAC_CONFIG_OUT_L
SCAC_CONFIG_IN_L
+2.5V_DIGITAL
RS_25 For SPAC2 chip RS_25 is 0 Ohm
SMLV2−
SMLV2+
SMLV1−
SMLV1+
MSLV2+
MSLV2−
MSLV1+
MSLV1−
SPAC bus signals
COMPANY:
NEVIS LABS–COLUMBIA UNIVERSITY
TITLE:
Atlas FEB – SPAC & CONFIG chip
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb/august/01
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET:
OF

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

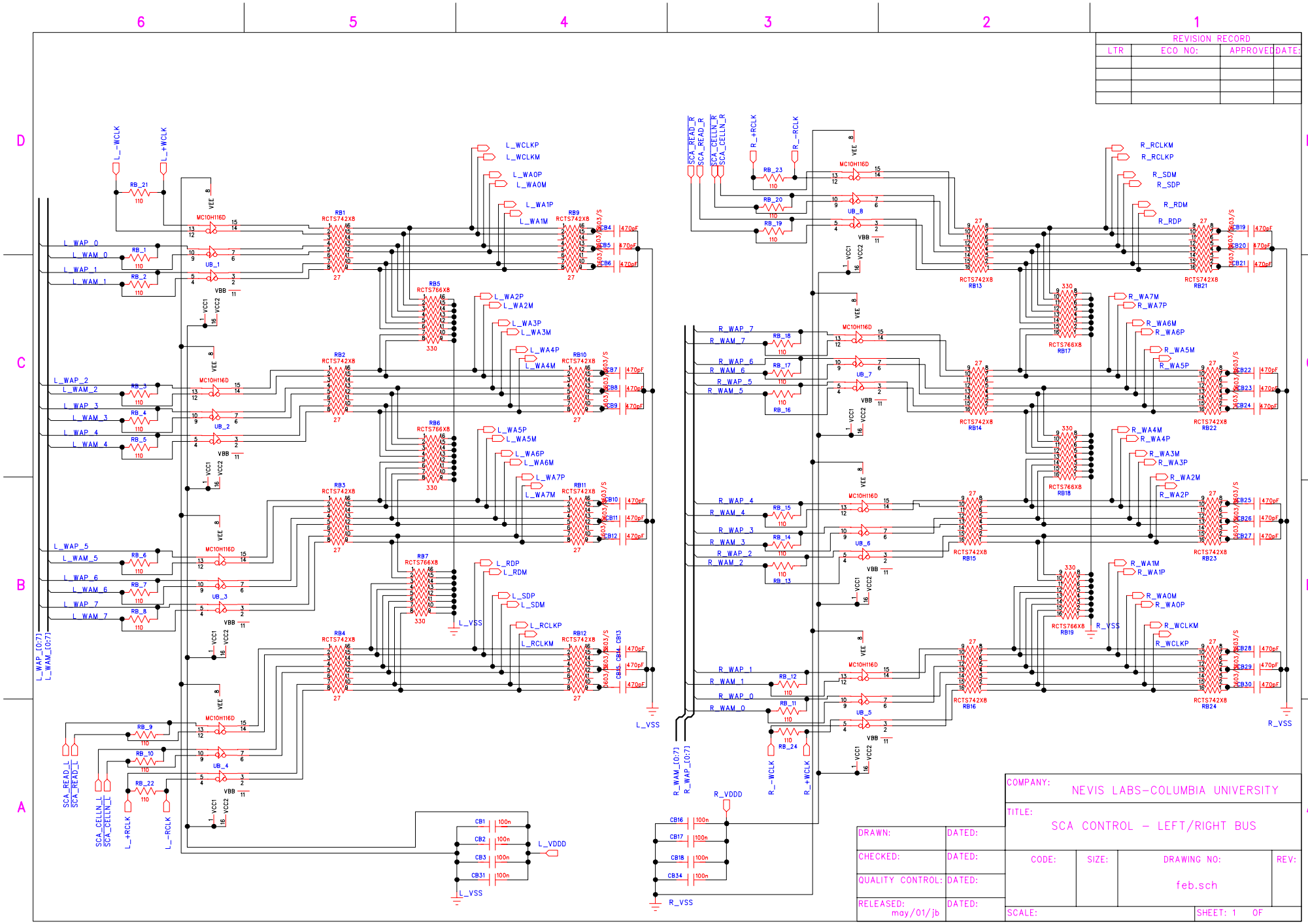


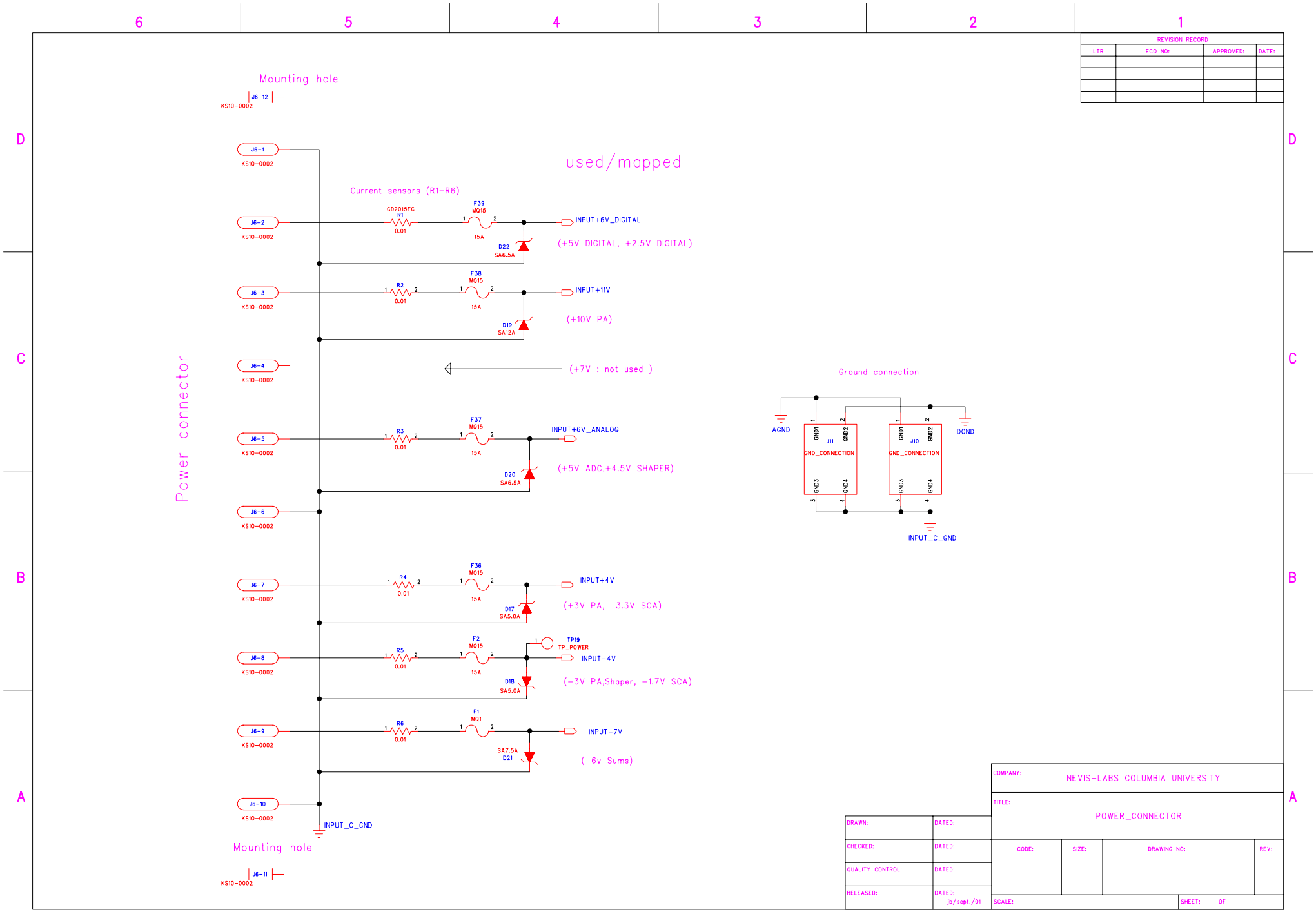
DRAWN:	DATED:	COMPANY: NEVIS-LABS COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: ATLAS FEB – TTCrx chip	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO:	REV:
RELEASED:	DATED: jb/august/01	SCALE:	SHEET: OF

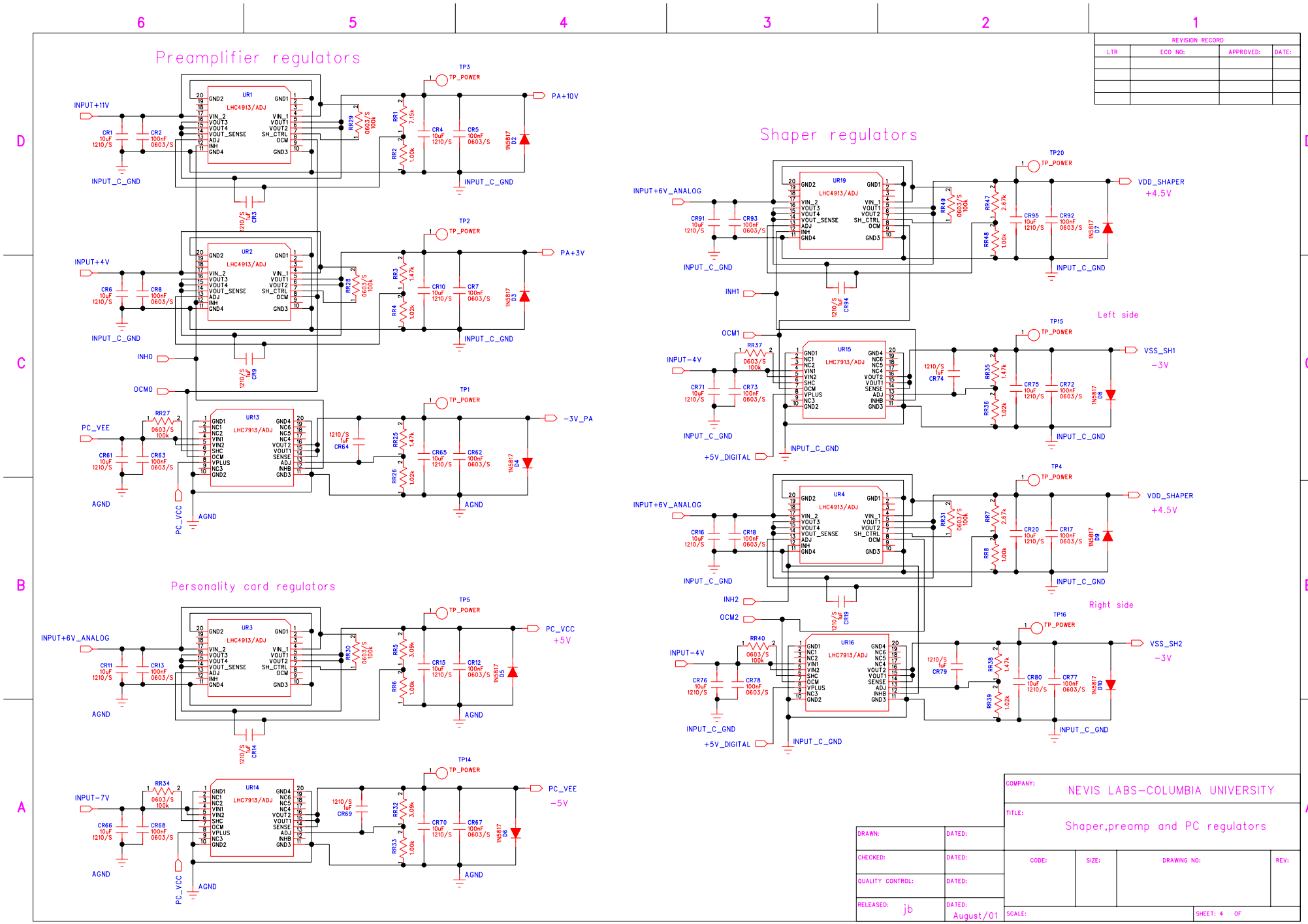


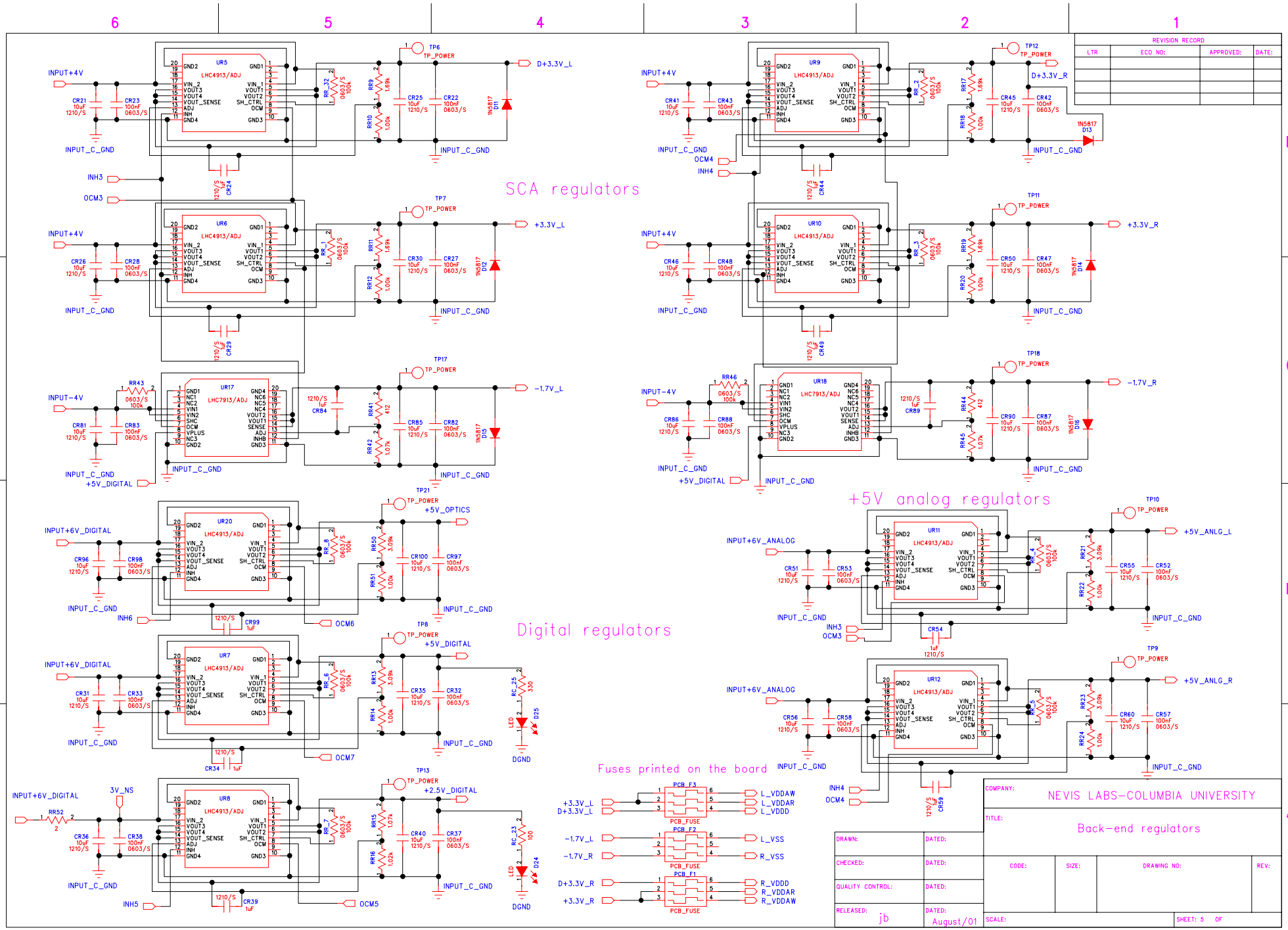
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

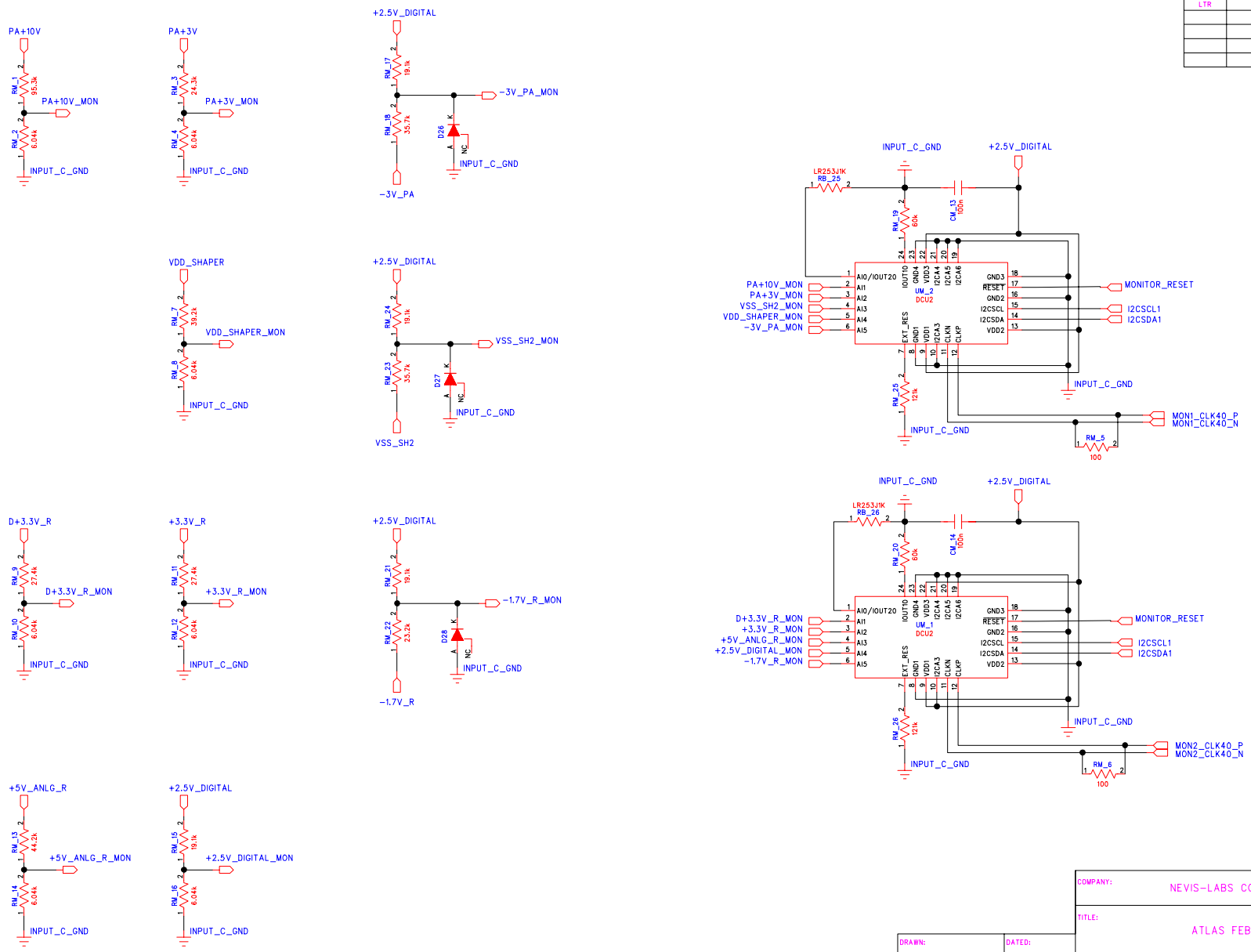
DRAWN:	DATED:	COMPANY: NEVIS-LABS COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: ATLAS FEB - clock distribution tree	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO:	REV:
RELEASED:	DATED: jb/august/01	SCALE:	SHEET: OF


REVISION RECORD
LTR
ECO NO:
APPROVED
DATE:
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
SCA CONTROL - LEFT/RIGHT BUS
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
may/01/jb
DATED:
CODE:
SIZE:
DRAWING NO:
feb.sch
REV:
SCALE:
SHEET: 1 OF
L_WAP_[0:7]
L_WAM_[0:7]
R_WAM_[0:7]
R_WAP_[0:7]
L_VSS
R_VSS
L_VDDD
R_VDDD


Mounting hole
J6-12
KS10-0002
J6-1
KS10-0002
used/mapped
Current sensors (R1-R6)
CD2015FC
R1
0.01
F39
MQ15
15A
INPUT+6V_DIGITAL
D22
SA6.5A
(+5V DIGITAL, +2.5V DIGITAL)
J6-2
KS10-0002
R2
0.01
F38
MQ15
15A
INPUT+11V
D19
SA12A
(+10V PA)
J6-3
KS10-0002
J6-4
KS10-0002
(+7V : not used)
Power connector
R3
0.01
F37
MQ15
15A
INPUT+6V_ANALOG
D20
SA6.5A
(+5V ADC,+4.5V SHAPER)
J6-5
KS10-0002
J6-6
KS10-0002
R4
0.01
F36
MQ15
15A
INPUT+4V
D17
SA5.0A
(+3V PA, 3.3V SCA)
J6-7
KS10-0002
R5
0.01
F2
MQ15
15A
TP19
TP_POWER
INPUT-4V
D18
SA5.0A
(-3V PA,Shaper, -1.7V SCA)
J6-8
KS10-0002
R6
0.01
F1
MQ1
INPUT-7V
SA7.5A
D21
(-6v Sums)
J6-9
KS10-0002
J6-10
KS10-0002
INPUT_C_GND
Mounting hole
J6-11
KS10-0002
Ground connection
AGND
DGND
GND1
GND2
GND3
GND4
J11
J10
GND_CONNECTION
INPUT_C_GND
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY:
NEVIS-LABS COLUMBIA UNIVERSITY
TITLE:
POWER_CONNECTOR
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
jb/sept./01
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET:
OF


Preamplifier regulators
Shaper regulators
Personality card regulators
Left side
Right side
INPUT+11V
INPUT+4V
INPUT+6V_ANALOG
INPUT-7V
INPUT-4V
PC_VEE
PC_VCC
INPUT_C_GND
AGND
INH0
OCM0
INH1
OCM1
INH2
OCM2
+5V_DIGITAL
PA+10V
PA+3V
-3V_PA
VDD_SHAPER
+4.5V
VSS_SH1
-3V
VSS_SH2
-3V
PC_VCC
+5V
PC_VEE
-5V
TP_POWER
LHC4913/ADJ
LHC7913/ADJ
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
Shaper,preamp and PC regulators
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb
August/01
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 4 OF

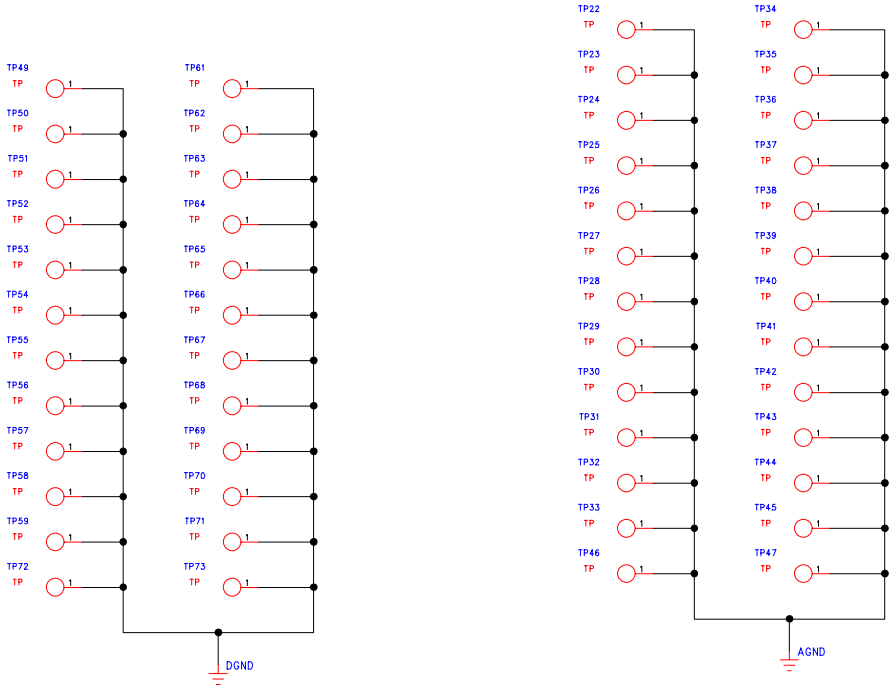

SCA regulators
+5V analog regulators
Digital regulators
Fuses printed on the board
UR5 LHC4913/ADJ
UR6 LHC4913/ADJ
UR17 LHC7913/ADJ
UR9 LHC4913/ADJ
UR10 LHC4913/ADJ
UR18 LHC7913/ADJ
UR20 LHC4913/ADJ
UR7 LHC4913/ADJ
UR8 LHC4913/ADJ
UR11 LHC4913/ADJ
UR12 LHC4913/ADJ
INPUT+4V
INPUT-4V
INPUT+6V_DIGITAL
INPUT+6V_ANALOG
INPUT_C_GND
+5V_DIGITAL
D+3.3V_L
+3.3V_L
-1.7V_L
D+3.3V_R
+3.3V_R
-1.7V_R
+5V_OPTICS
+2.5V_DIGITAL
+5V_ANLG_L
+5V_ANLG_R
3V_NS
DGND
PCB_F3
PCB_F2
PCB_F1
PCB_FUSE
L_VDDAW
L_VDDAR
L_VDDD
L_VSS
R_VSS
R_VDDD
R_VDDAR
R_VDDAW
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY:
NEVIS LABS-COLUMBIA UNIVERSITY
TITLE:
Back-end regulators
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
jb
August/01
CODE:
SIZE:
DRAWING NO:
REV:
SCALE:
SHEET: 5 OF



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

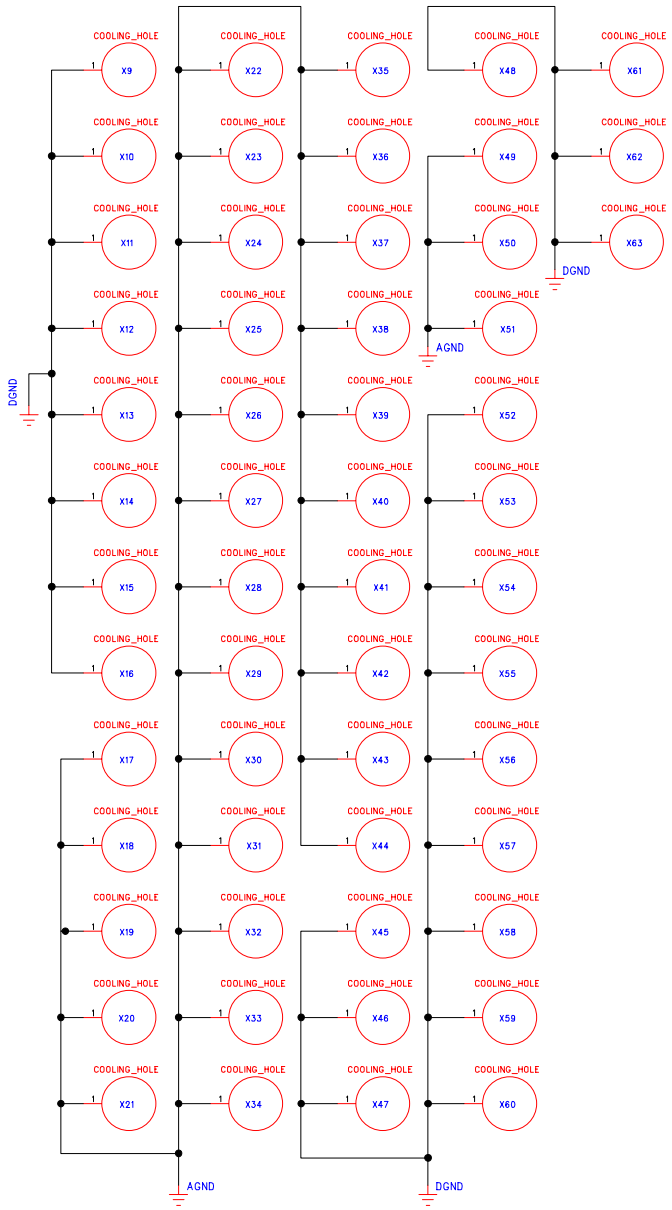
DRAWN:	DATED:	COMPANY: NEVIS-LABS COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: ATLAS FEB - Monitor chips	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO:	REV:
RELEASED: jb/01	DATED: oct./01	SCALE:	SHEET: OF

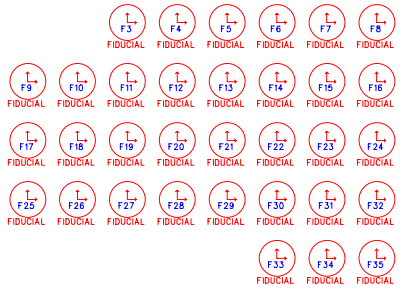
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

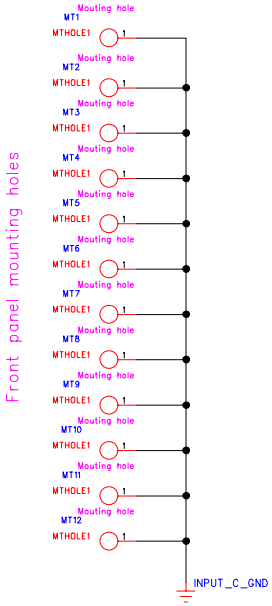


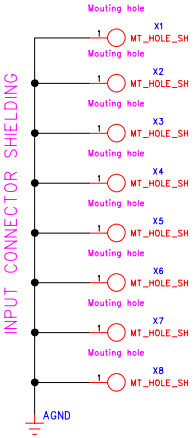
		COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY			
		TITLE: ATLAS FEB – test points			
DRAWN:	DATED:				
CHECKED:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
QUALITY CONTROL:	DATED:				
RELEASED: jb/sept/01	DATED:	SCALE:		SHEET: OF	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

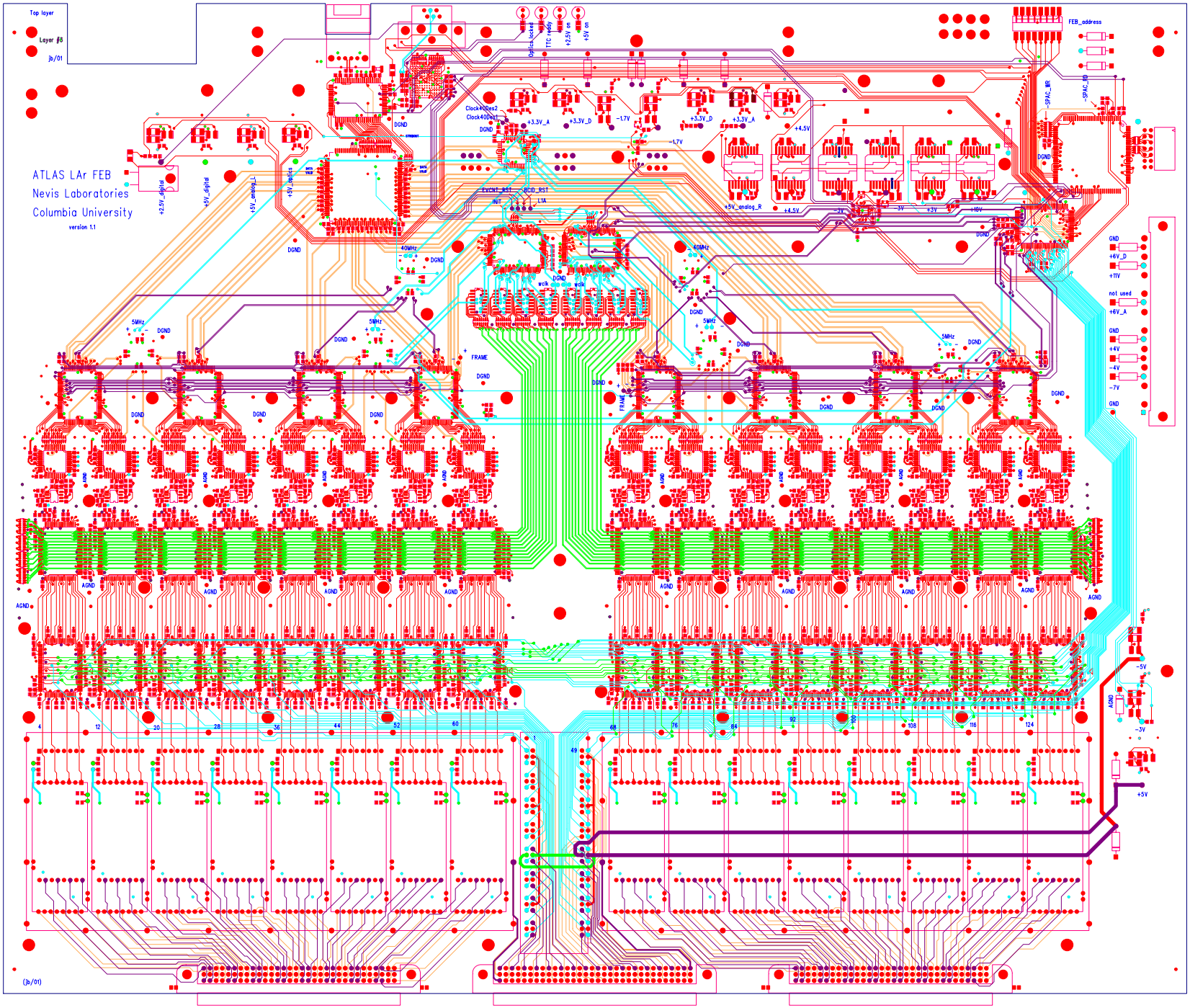


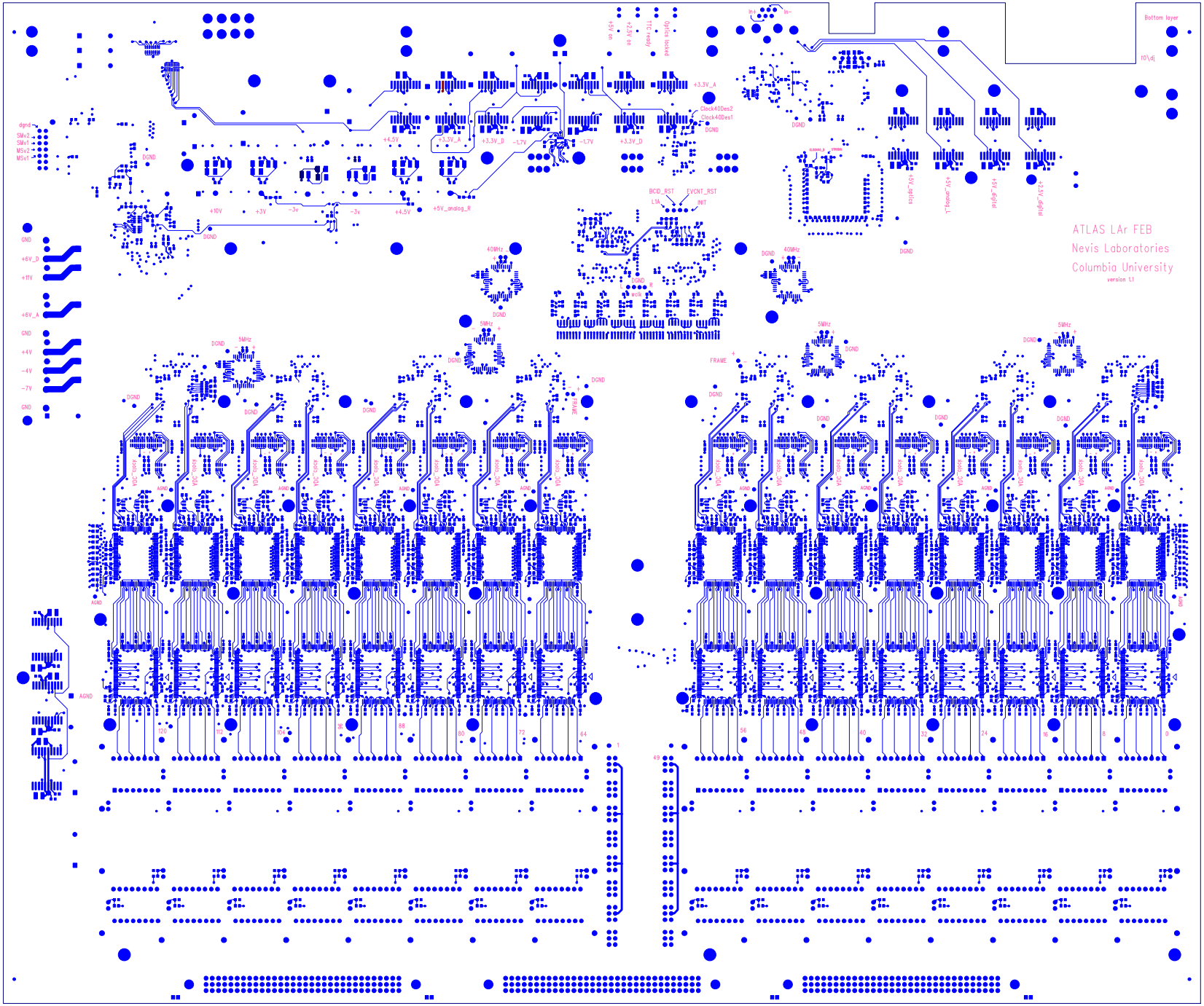






DRAWN:	DATED:	COMPANY: NEVIS LABS-COLUMBIA UNIVERSITY	
CHECKED:	DATED:	TITLE: Mounting and cooling holes, fiducials	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO:	REV:
RELEASED: jb	DATED: august/01	SCALE:	SHEET: OF


Top layer
Layer #8
jb/01
ATLAS LAr FEB
Nevis Laboratories
Columbia University
version 1.1
FEB_address
Optical_clock
TTC_reset
+2.5V on
+5V on
Clock40Des2
Clock40Des1
+3.3V_A
+3.3V_D
-1.7V
+4.5V
+5V_analog_R
+2.5V_digital
+5V_digital
+5V_analog
+5V_digital
-SPAC_MR
-SPAC_DR
DGND
AGND
40MHz
5MHz
EVCNT_RST
BCID_RST
INIT
L1A
FRAME
wclk
GND
+6V_D
+11V
not used
+6V_A
+6V
-6V
-7V
-5V
-3V
+5V
(jb/01)


ATLAS LAr FEB
Nevis Laboratories
Columbia University
version 1.1
Bottom layer
dgnd
SMv2
SMv1
MSv2
MSv1
GND
+6V_D
+11V
+6V_A
+4V
-4V
-7V
+10V
+3V
-3v
+4.5V
+5V_analog_R
+3.3V_A
+3.3V_D
-1.7V
Clock40Des2
Clock40Des1
DGND
BCID_RST
EVCNT_RST
L1A
INIT
40MHz
5MHz
FRAME
AGND
+5V_analog_L
+5V_digital
+2.5V_digital
+1.5V_analog
Vdd_VDA
Vdd_VDD
Vdd_VDA
Vdd_VDD
120
112
104
96
88
80
72
64
56
48
40
32
24
16
8
0
1
49

Layer definition (proposition) for Atlas-FEB

nov. 97
v1.28

Layer/Area	Input connector	Preamplifier and Shaper	SCA and ADC	Digital		
Layer 1	AGND	Routing	Routing	Routing		Top 0.7
Layer 2	AGND		AGND	DGND	P	4.7 1.3
Layer 3	Input signals routing	Trigger out −3V	VSS	Output signal routing	C	12.0 1.3
Layer 4	AGND		VDDAW VDDD VDDAR	DGND	P	3.8 1.3
Layer 5		Trigger routing(in)	VSS +5.5V	+5V_ADC +3.3V Routing	C	6 1.3
Layer 6		PA +10V,+3V,CALIB Shaper control	VSS Digital bus VSS	+5V	P	6 1.3
Layer 7	AGND		VDDAW VDDD VDDAR	DGND	C	6 1.3
Layer 8	Input signals routing	Trigger out +4.5V	VSS	Routing	P	3.8 1.3
Layer 9	AGND		AGND	DGND	C	12.0 1.3
Layer 10	AGND	Routing	Routing	Routing	P	4.7 0.7 Bottom

total: 70.8 mils