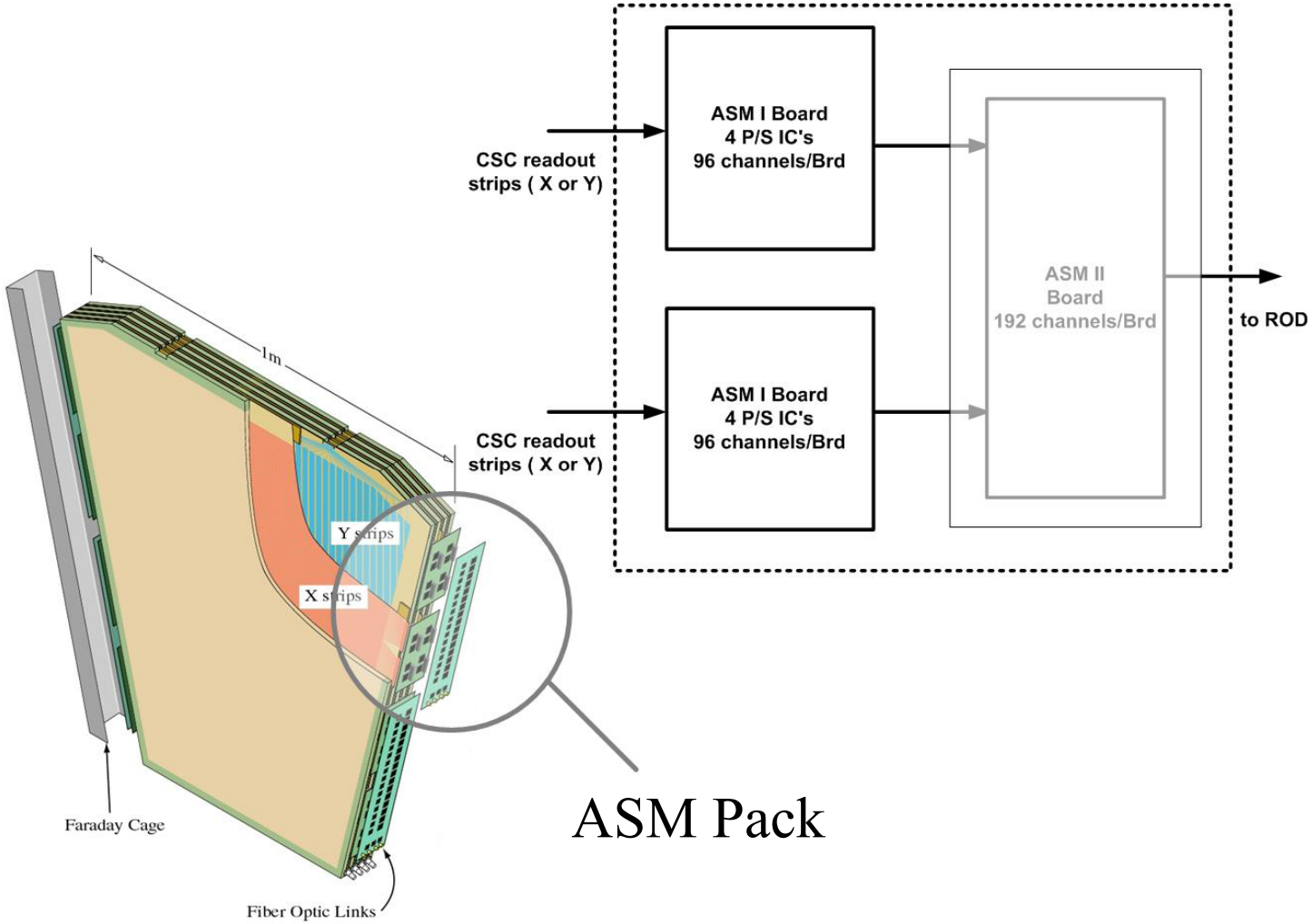
# ATLAS CSC
# Front-End Electronics PRR
# ASM1

Anand Kandasamy

# CSC Chamber and Electronics



# Amplifier Storage Module (ASM) 1

- Each ASM1 handles 96 CSC signals
- Contains
  - Four custom Preamplifier/Shaper ASIC
  - One CERN LHC Positive Voltage Regulator
  - ESD Protection Circuitry
- 960 Channels/Chamber (X: 768, Y:192)

# CSC Preamplifier/Shaper ASIC

- 0.5 μm 3.3V CMOS Process
  - Agilent Technologies
  - Single Poly with Silicide block for poly resistors
  - Triple metal routing
  - High-density, linear MOS capacitor (2.2 fF/um2)
- Reputed and Tested to be RADHARD

# ASIC Development Roadmap

| | | |
|---|---|---|
| IC50 Initial Prototype | 16 Channels/Die/45% yield | May-99 |
| Internal Review | BNL/J. Oliver | June-99 |
| Test Beam at X5 | | October-99 |
| IC50 TID Test | BNL/GIF | February-00 |
| IC50 Refab (same mask) | 80 pin EDQUAD/97% yield | February-00 |
| Conceptual Design Review | BNL/ B. Cleland, J. Parsons, R. Van Berg, H. Gordon and L. Premisler | August-00 |
| IC50 Refab (same mask) | 80 pin EDQUAD/84% yield | January-01 |
| Front End Elec. Review | Boston/ Status of the Front End Electronics for the ATLAS Cathode Strip Chambers | May-01 |
| IC71 | 25 Channels/100 pins/100% yield | July-01 |
| IC71 Spares | 96% yield | January-02 |
| IC71 TID test | BNL/GIF | March-02 |
| Test Beam at X5 | | August-02 |
| IC71 spares | Package change/ 100pin QFP/98.7% yield | September-02 |
| Final Design Review | BNL/ B. Cleland, J. Parsons, M. Newcomer, J. Oliver and L. Premisler | December-02 |
| NIEL Test | Prospero | April-03 |
| Single Event Upset Test | MGH | May-03 |
| ASIC PRR | BNL/P. Farthouat, F. Anghinolfi, J. Parsons, M. Newcomer and L. Premisler | July-03 |
| Fabrication Begin | | October-03 |
| Fabrication Complete | | March-04 |

# IC50 Redesigned

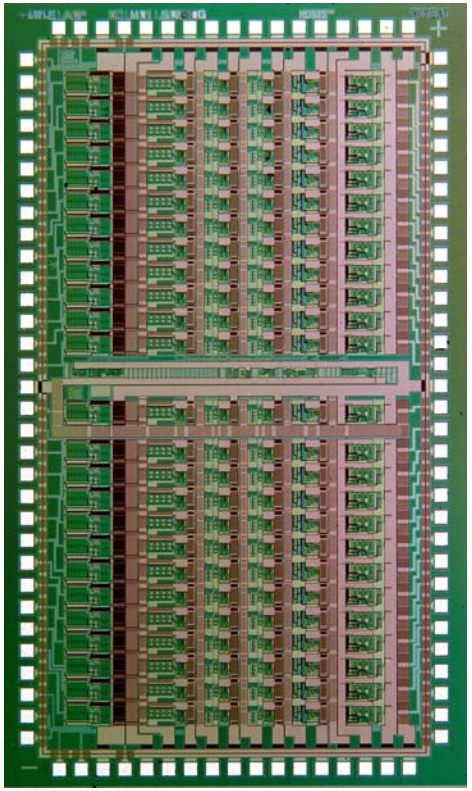
- Redesign - Layout
  - Layout scrubbed and large capacitors on bias lines removed
  - MOSIS was asked to perform Design Rule Check on the mask to identify potential violations.
  - DRC report from MOSIS was used to scrub the layout of any DRC violations.
- Redesign – Functional
  - Lower input impedance
  - Improved overload recovery
  - Channel count increased to 25 (24 active and 1 reference)

# IC71 prototyping results

- Basic performance specifications unchanged from IC50
- Improved overload recovery
- Improved yield (98.4%) with no bias circuit failures observed.
- Packaging
  - Devices were packaged in cavity down, thermally enhanced EDQUAD package.
  - MOSIS switched packaging vendor from ASAT to OSE-USA. EDQUAD package was not available. Switched to cavity up PQFP

# IC71 CSC Preamplifier/Shaper

| | |
|---|---|
| Technology | 0.5 µm CMOS |
| Channels | 25 |
| Die size | 3.29 x 5.79 mm |
| Architecture | Single-ended |
| Intended Cdet | 20 – 100 pF |
| Input device | NMOS W/L = 5000/0.6 µm, Id = 4mA |
| Noise | 1140 + 17.6 e-/pF |
| Gain | 3.8 mV/fC |
| Max. linear charge | 450 fC |
| Class AB Output swing | To power supply - 250 mV |
| Pulse shape | $7^{th}$ order complex Gaussian, bipolar |
| Pulse peaking time, 5% - 100% | 73 ns |
| FWHM | 340 ns |
| Max. output loading (3% distortion) | 500 Ω, 500 pF |
| Crosstalk | 0.8% adjacent, 0.5% non-adjacent |
| Power supply | Single +3.3V |
| Power Dissipation | 32.5 mW/chan |



# ASIC PRODUCTION COMPLETED

- Total Preamp/Shaper IC's for ATLAS CSC's
  - 2560 for 64 chambers + 10% spares
- Production Lot
  - 20 Wafers Cut and Packaged into 100 pin QFP
  - 7220 packaged parts obtained
- An yield of 39% will be sufficient, but history with this process indicates yield numbers in the upper 90's

# ASIC Testing

- All Preamplifier/Shaper will be tested using a custom built IC tester.
- IC's will be identified as follows

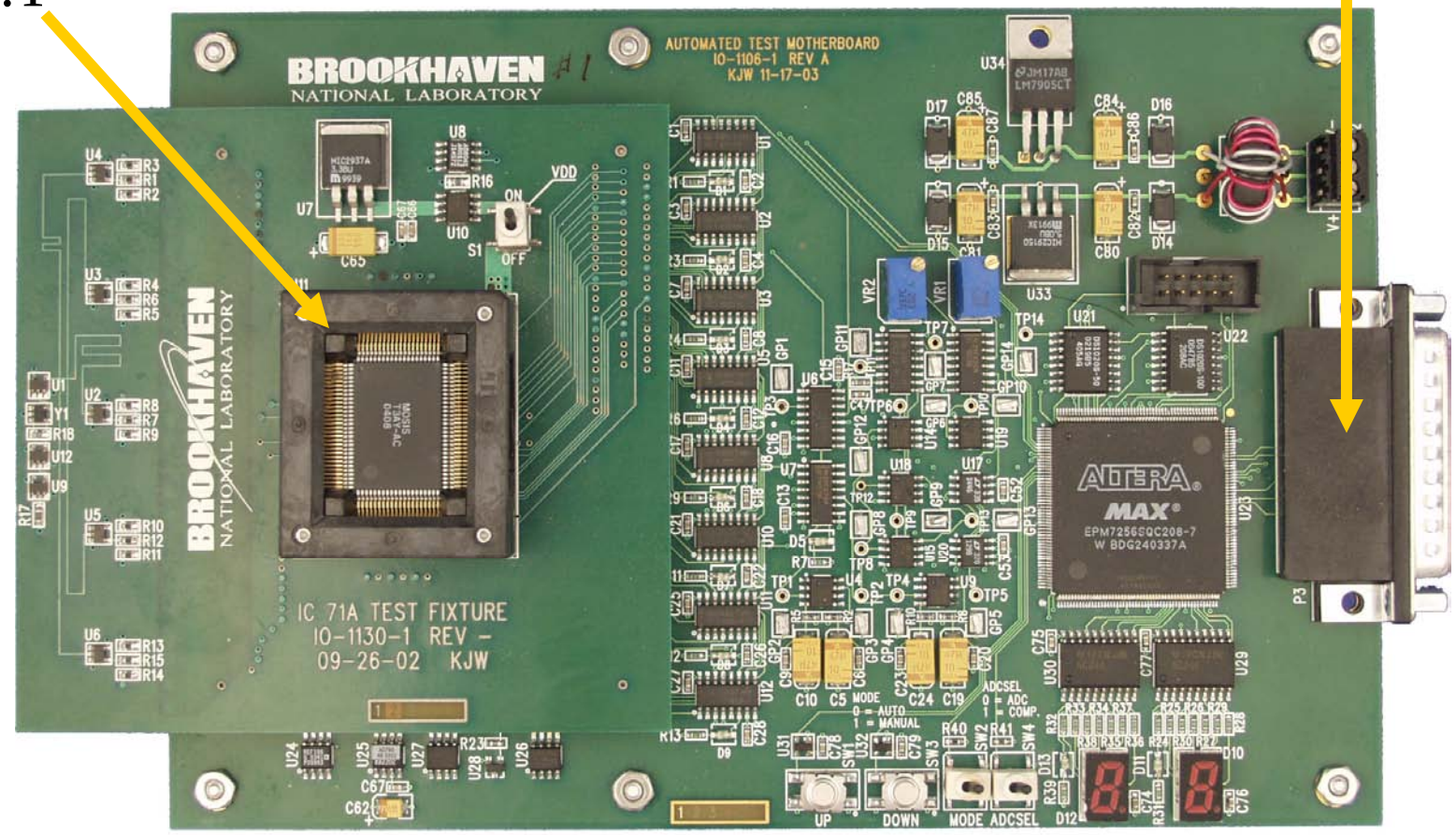
  BOX# + TRAY# + ROW + COL

- IC's will not tracked for the entire system
  - modularity stops at the PC board level.

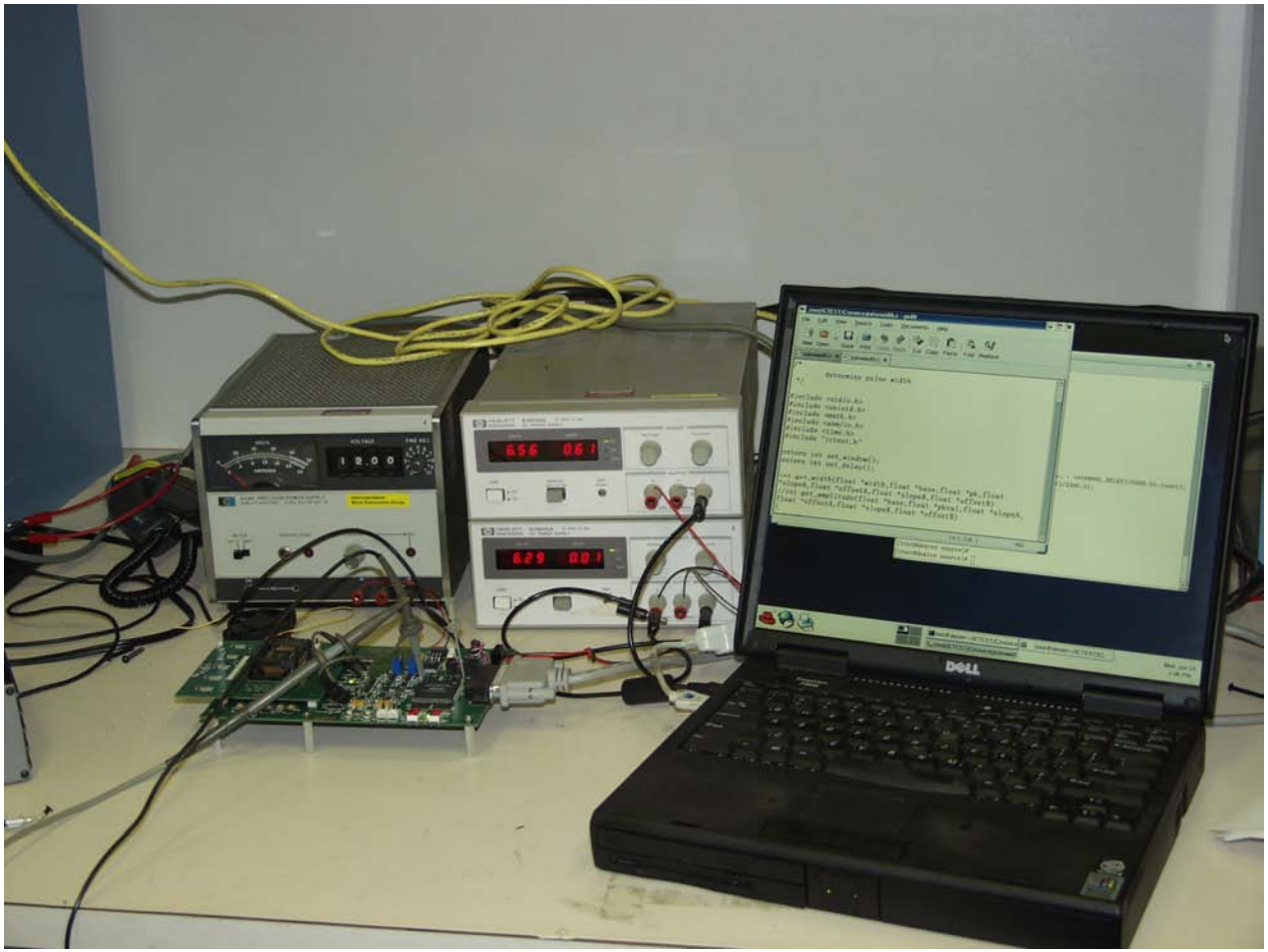
# ASIC Tester

D.U.T

Parallel Port Interface



# Preamp/Shaper Test Setup

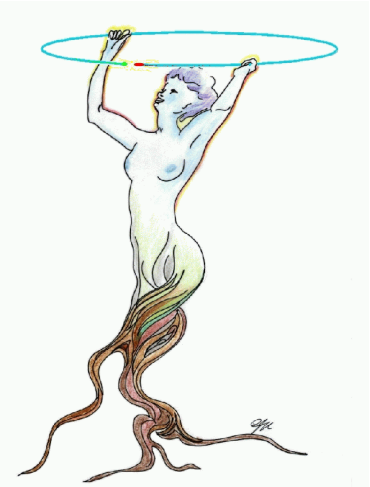


- IC Tester
- Linux Computer with network connection
- Database Server
- Dual Power Supplier
- Human to change test devices

Test Time: 21 seconds

# Database & Analysis

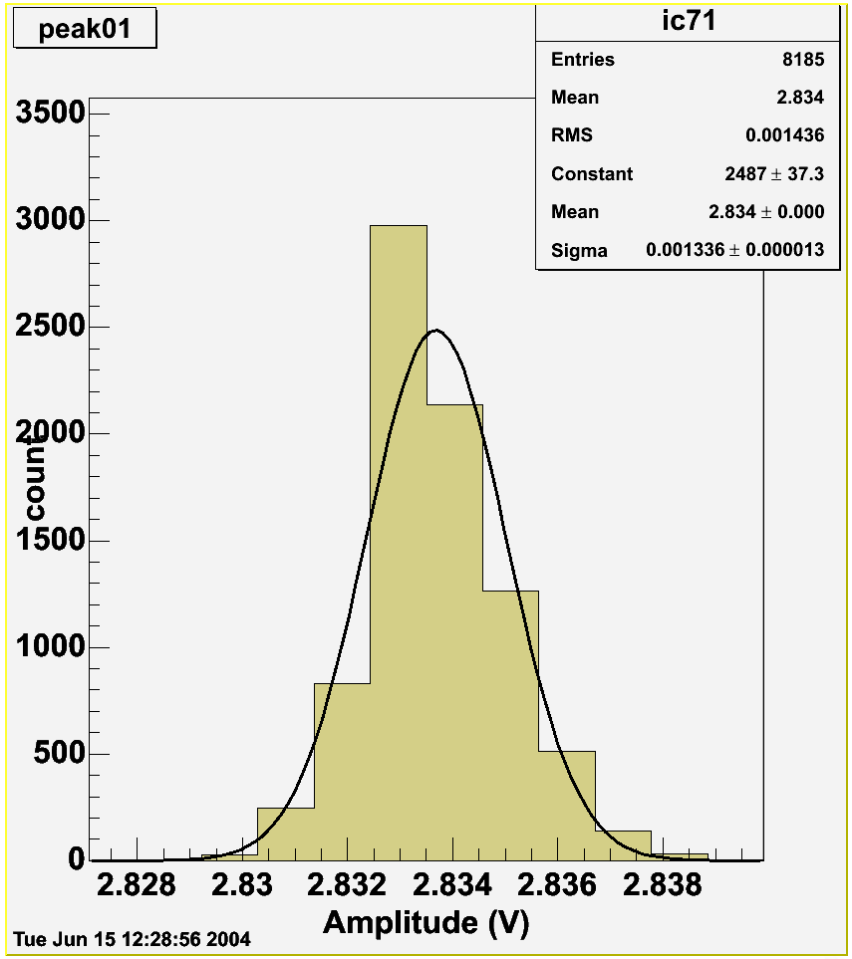
- Parameters stored in DB
  - Baseline
  - Noise
  - Amplitude
  - Pulse Width @ 50% of pulse height
  - Bias voltages
  - Current consumption by D.U.T
  - Chip ID



# IC Tester output

```
./ictest
Enter Box Number:1
Enter Tray Number:2
ADC   Slope: 0.9976270 Offset: 0.0002 V
DAC A Slope: 0.9951019 Offset: 11.5838 mV
DAC B Slope: 0.9954864 Offset: 5.4339 mV
Enter Row Number:3
Enter Col Number:4
Serial number: 01-002-03-4
*********************************************************************
Chan   Base    noise    ampl   pwidth |   Bias voltages
*********************************************************************
Ch  0: 1.8796 [0.00098] 2.8525 66.938 | Bias  0 1.95173 [0.00499]
Ch  1: 1.8773 [0.00104] 2.8840 66.938 | Bias  1 0.87259 [0.00057]
……................
Ch 10: 1.9155 [0.00086] 2.9275 68.813 | Bias 10 0.11476 [0.00030]
Ch 11: 1.8915 [0.00079] 2.9190 66.313 | Bias 11 1.70895 [0.00075]
Ch 12: 1.8863 [0.00083] 2.9330 68.188 | Bias 12 1.44213 [0.00070]
……................
Ch 15: 1.9067 [0.00105] 2.8835 66.938 | Bias 15 0.63719 [0.00029]
……................
Ch 23: 1.8777 [0.00069] 2.9045 66.938 |
Ch 24: 1.8886 [0.00089] 2.8350 66.313 | IDD: 230.65
Elapsed Time 21 seconds
*********************************************************************
```

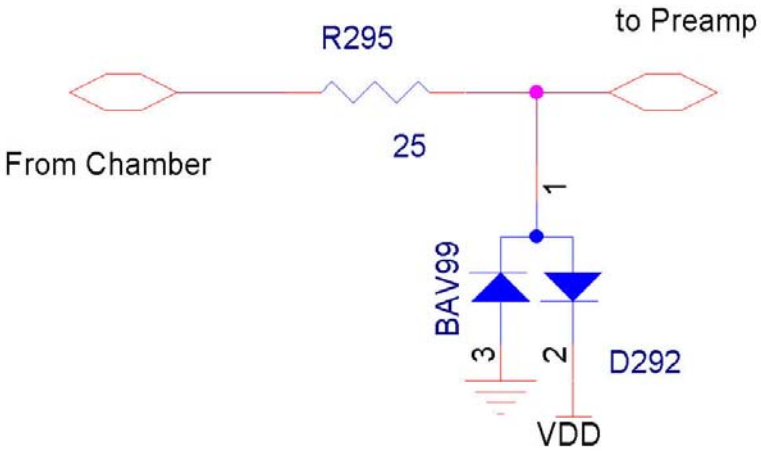
**Generated using Root scripts**



# ASM1 Board Status

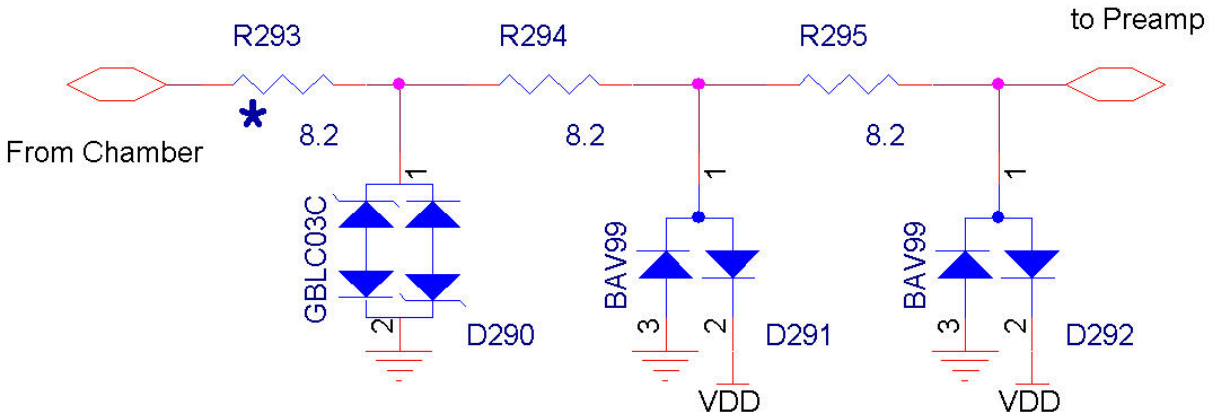
- New layout to add additional ESD protection circuitry.
- The need for the additional ESD protection devices (4 components/ch) was determined a month ago.
- Tests were conducted to determine the robustness of this new ESD protection and was found to be functioning.
- Total components added, introduced additional complexity in board design.

# Changes to ASM1

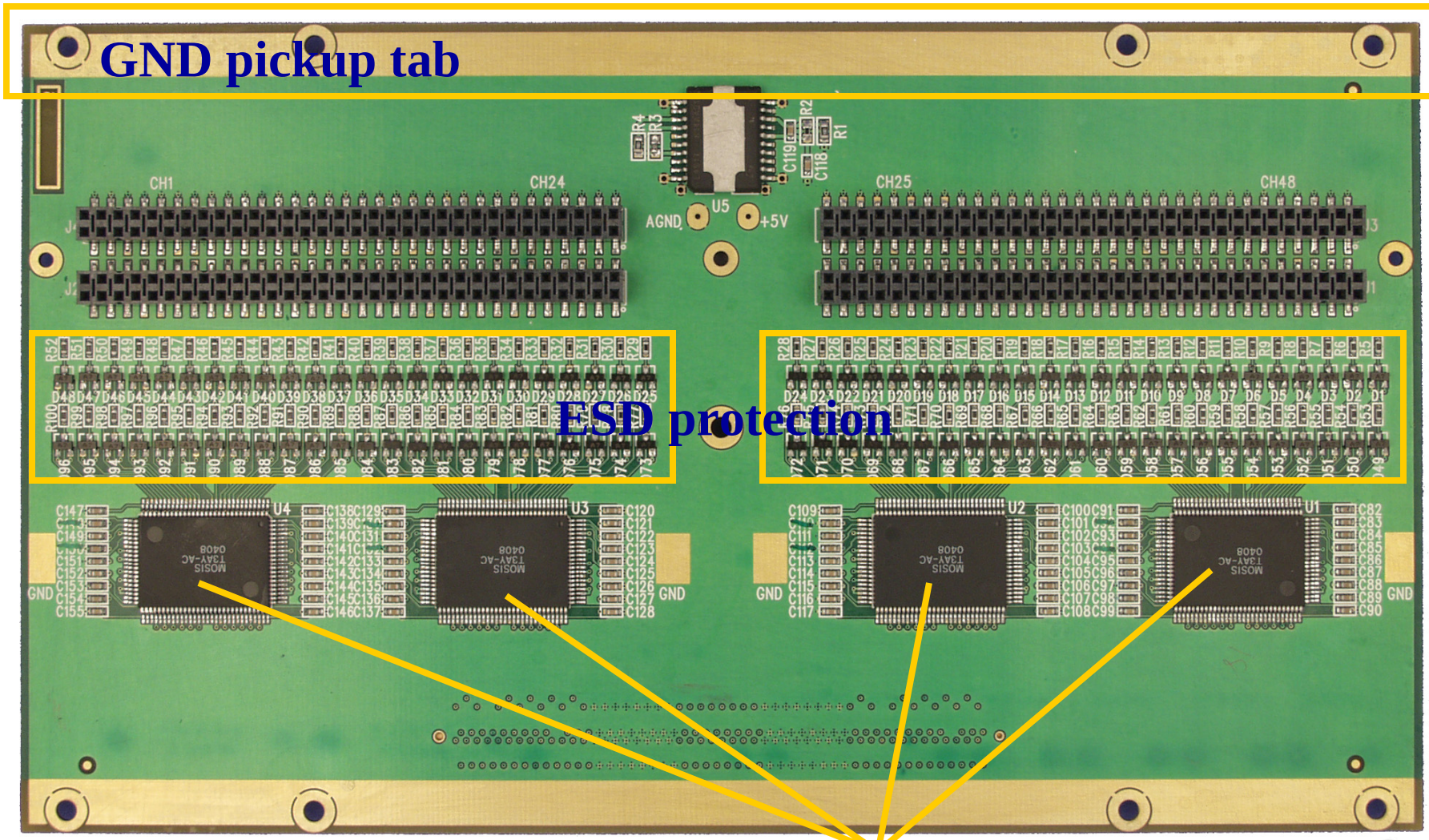



**REV. B**

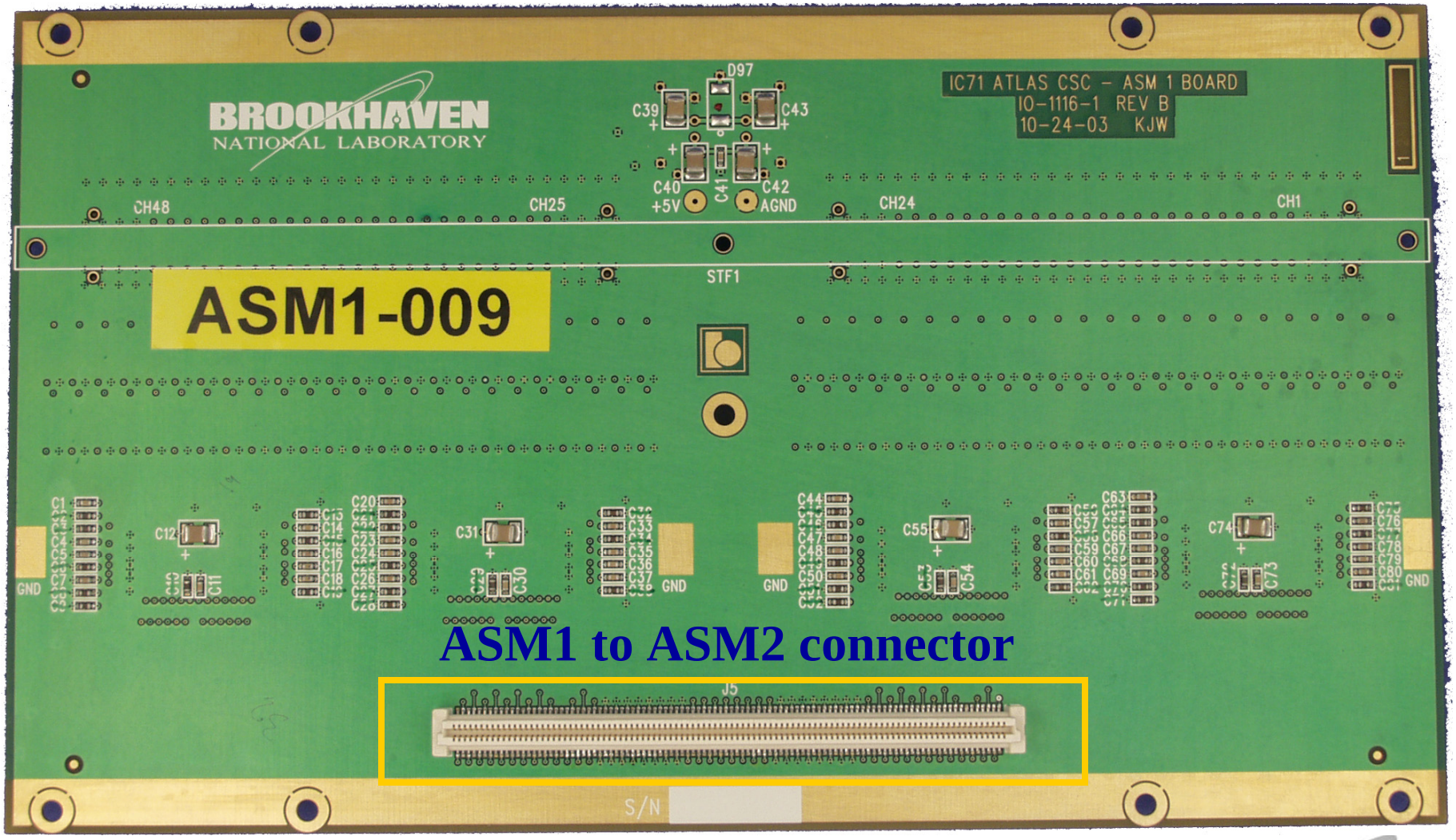
**REV. C**



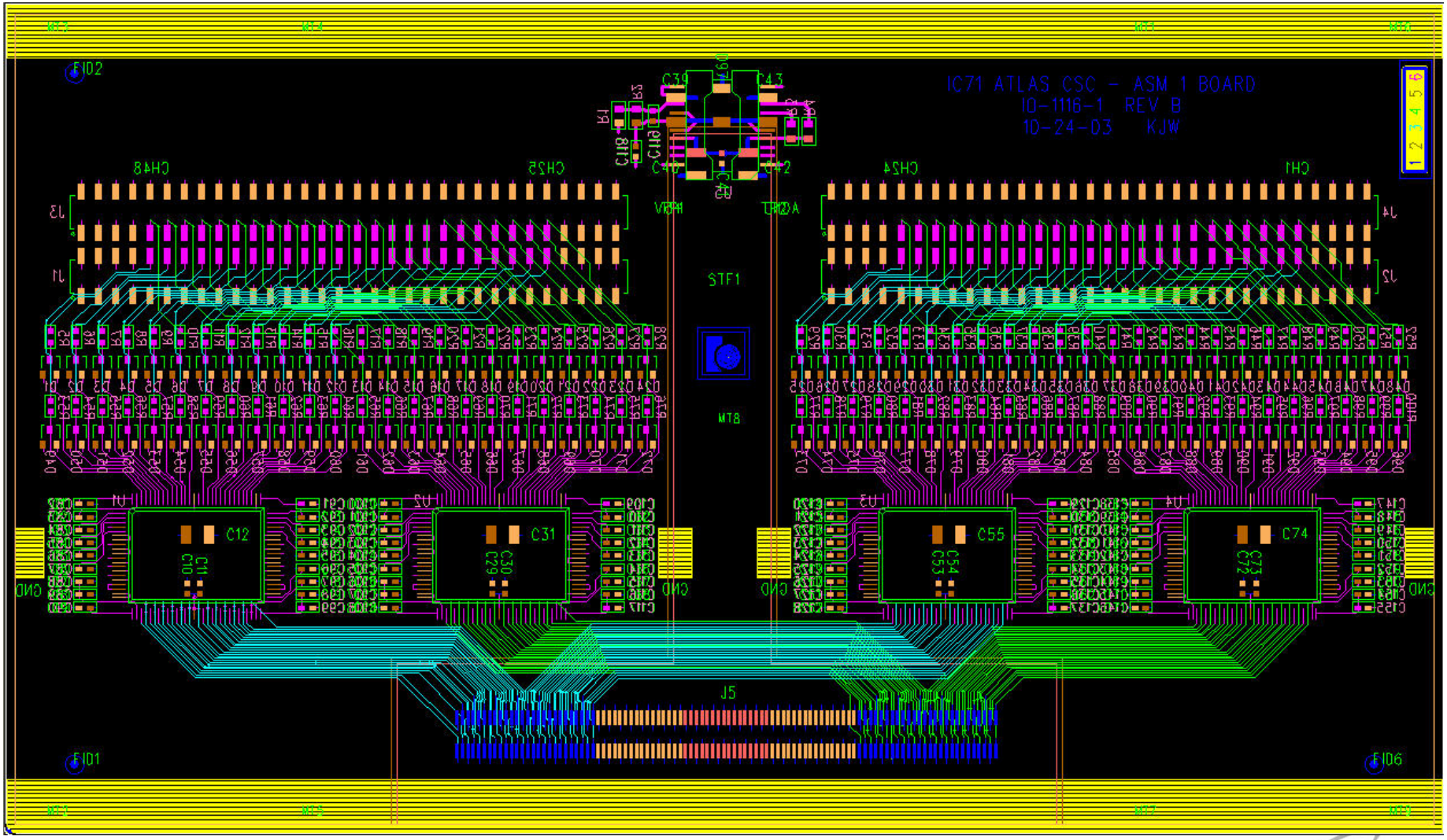
# ASM1 Rev. B (bottom)



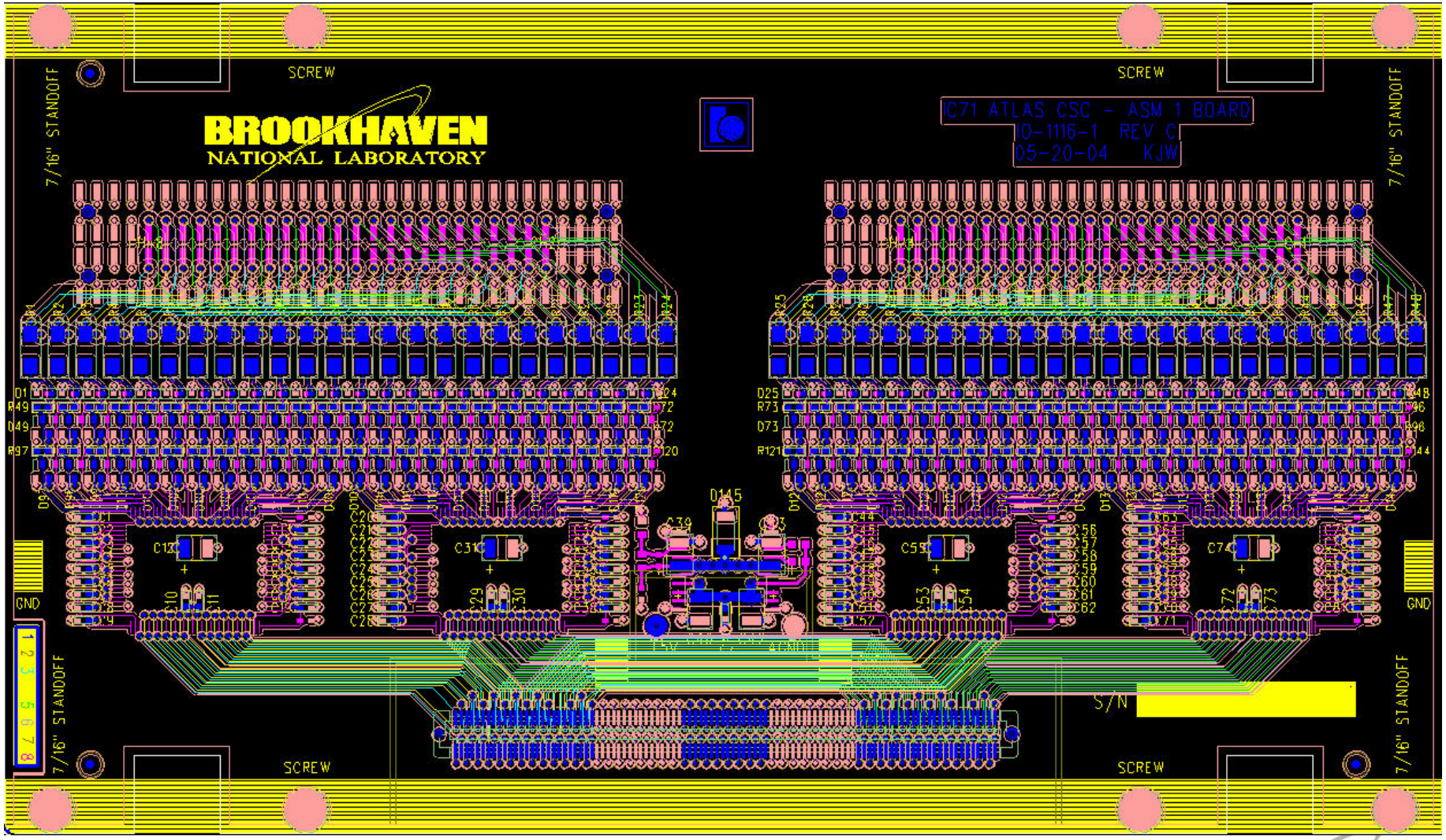
# ASM1 Rev. B (top)



# ASM1 Rev B



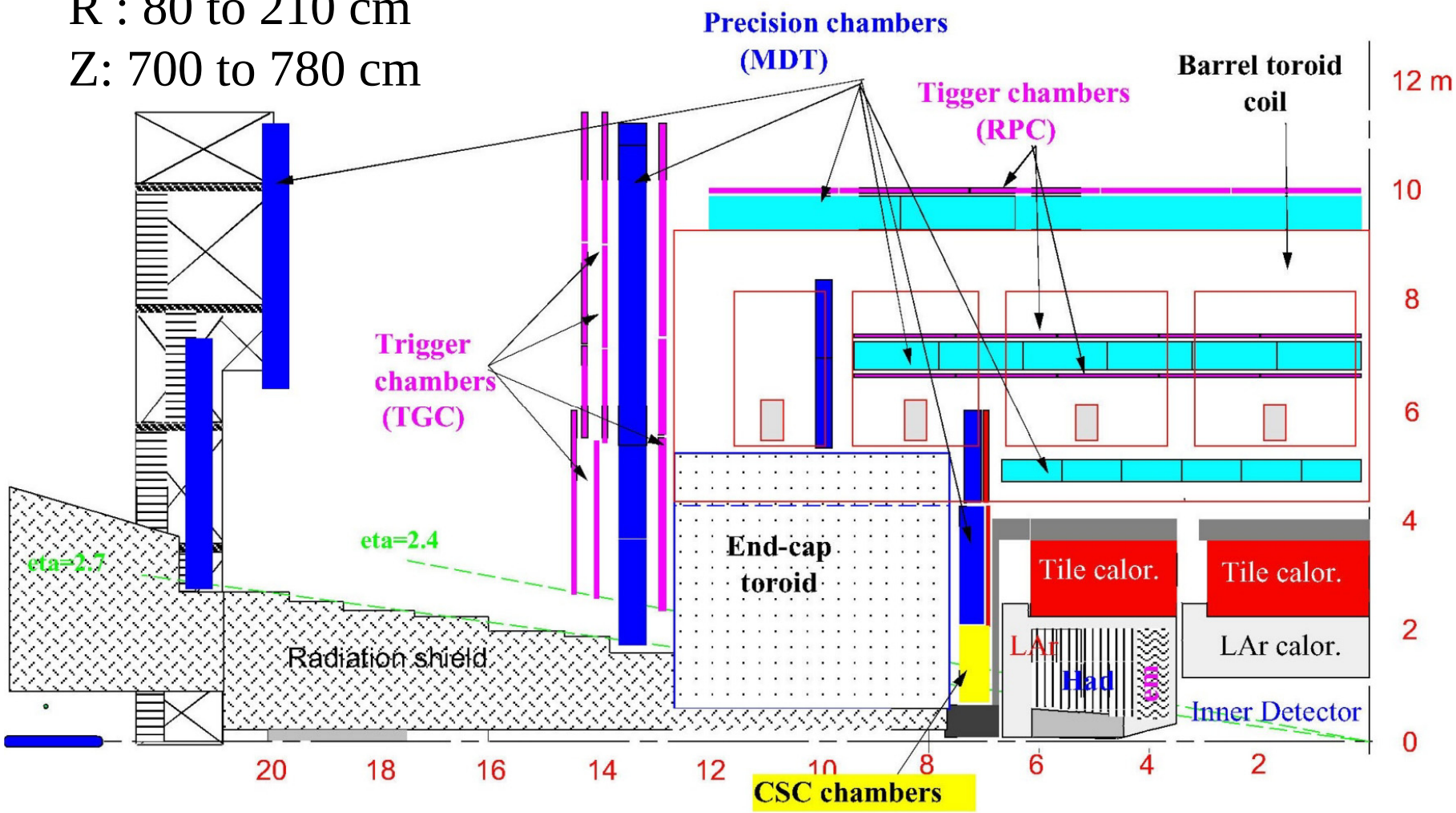
# ASM1 Rev. C Production Layout



# CSC Location in ATLAS

R : 80 to 210 cm

Z: 700 to 780 cm



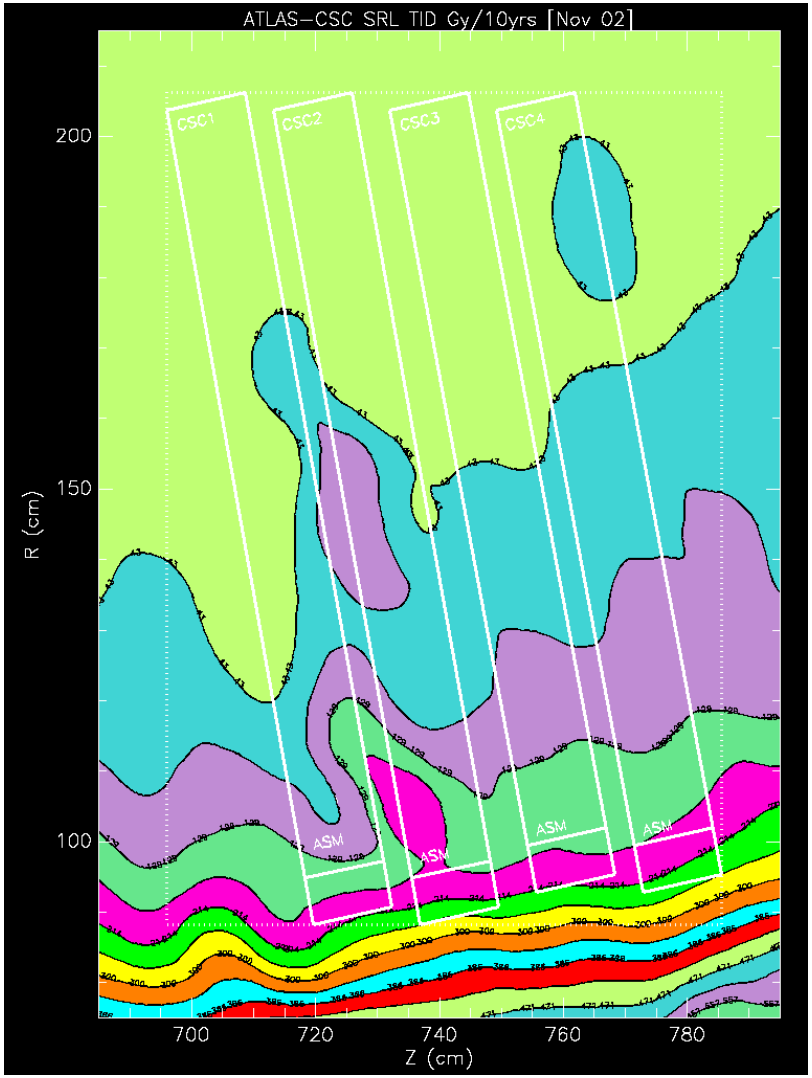
# Worst Case Radiation Levels in CSC

| TEST | SRL | RTC Pre-sel. | RTC Qual. |
|---|---|---|---|
| TID (KRad/10years) | 24.3 | 850.5 | 425.3 |
| NIEL (1 MeV eq $n.cm^{-2}$/10years) | $7.1 \times 10^{12}$ | $7.1 \times 10^{13}$ | $3.55 \times 10^{13}$ |
| SEE/SEU (>20 MeV $h.cm^{-2}$/10years) | $1.52 \times 10^{12}$ | $1.52 \times 10^{13}$ | $7.6 \times 10^{12}$ |

# Radiation Levels CSC Vs. LAr

| TEST | SRL | RTC Pre-sel. | RTC Qual. |
|---|---|---|---|
| TID (KRad/10years) | 24.3 | 850.5 | 425.3 |
| | 5 | 170 | 87.5 |
| NIEL (1 MeV eq n.cm$^{-2}$/10years) | $7.1 \times 10^{12}$ | $7.1 \times 10^{13}$ | $3.55 \times 10^{13}$ |
| | $1.6 \times 10^{12}$ | $1.6 \times 10^{13}$ | $8.0 \times 10^{12}$ |
| SEE/SEU (>20 MeV h.cm$^{-2}$/10years) | $1.52 \times 10^{12}$ | $1.52 \times 10^{13}$ | $7.6 \times 10^{12}$ |
| | $7.7 \times 10^{11}$ | $7.7 \times 10^{12}$ | $3.8 \times 10^{12}$ |

# TID Contour map for CSC

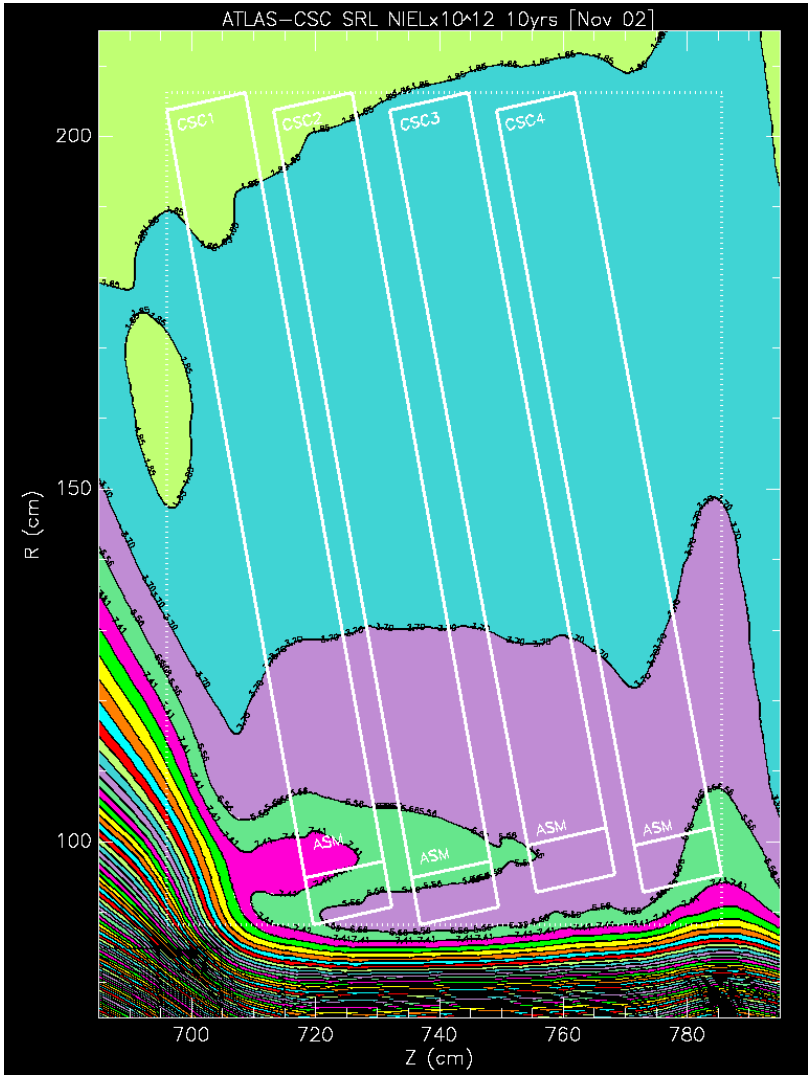



- CSC Electronics are located in the region where total TID achieved over 10 years is

**2 KRad << TID << 17.1 KRad**

4.3 KRad contour steps
Start: 55.7KRad
End: 4.3KRad

# 1 MeV eq. Neutrons Contour map for CSC

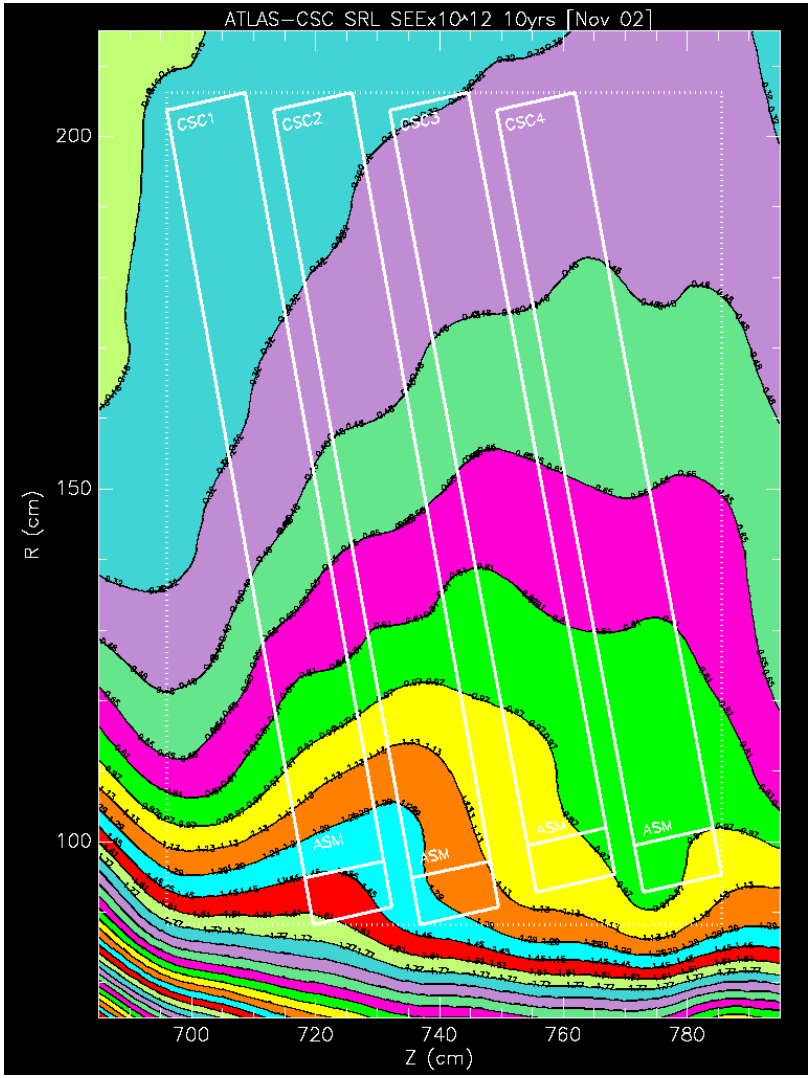



- CSC Electronics are located in the region where total NIEL fluence achieved over 10 years is

$$1.5\times10^{12} << \text{NIEL} << 7.4\times10^{12}$$

$1.85\times10^{12}$ contour steps
Start: $1.48\times10^{14}$
End: $1.85\times10^{12}$

# >20 MeV Hadron Contour map for CSC




- CSC Electronics are located in the region where total hadron fluence achieved over the course of 10 years is

$1.6\times10^{11} << SEE << 1.5\times10^{12}$

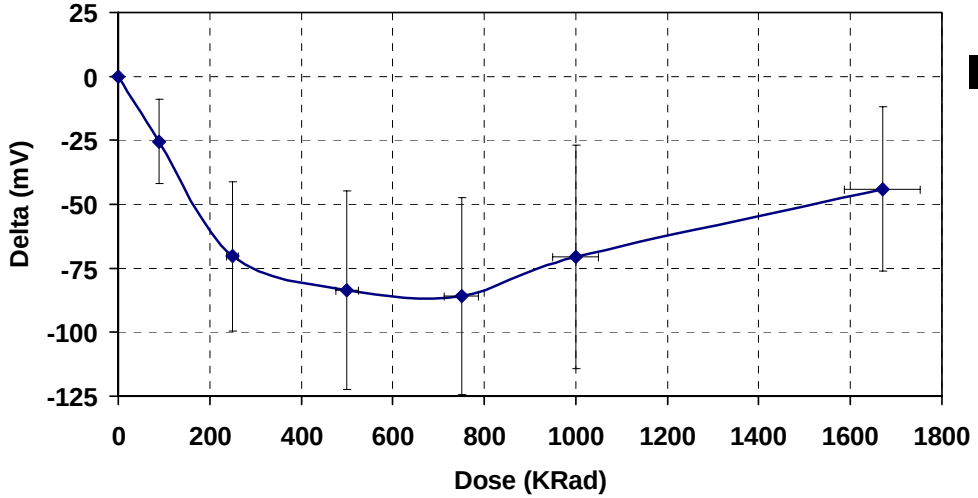
$1.6\times10^{11}$ contour steps
Start: $4.8\times10^{12}$
End: $1.6\times10^{11}$

# TID Test Results – Preamp/Shaper

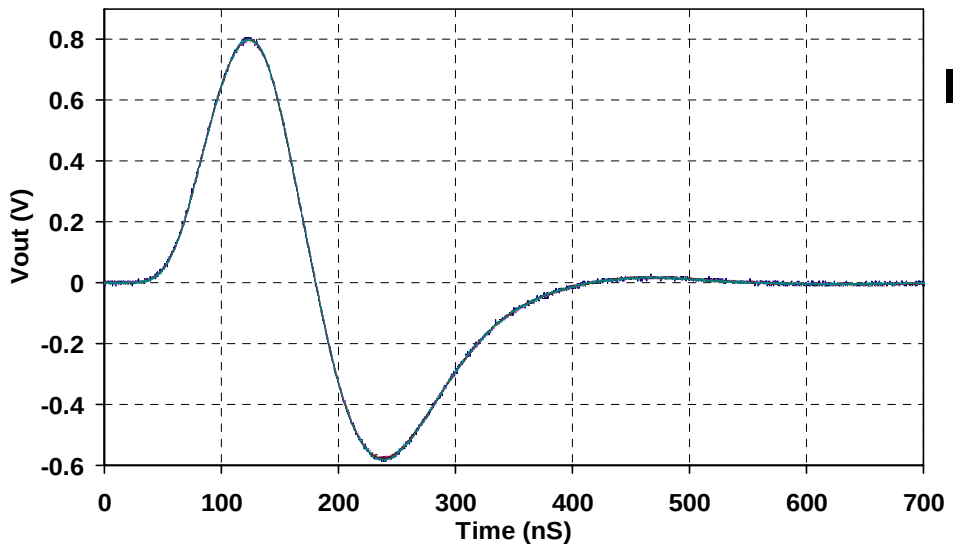
- CSC Preamp/Shapers ASIC was irradiated at the $^{60}$Co source in BNL to 1.67 MRad
- 150 Channels Observed with no failures or significant changes in their specifications

| Parameter | % Change from Pre-Radiation Measurement |
|---|---|
| Charge Gain | 0.44% |
| Shaping Time | 1.79% |
| ENC | 7.43% |
| Device Current | 1.39% |

# TID Test Results – Preamp/Shaper

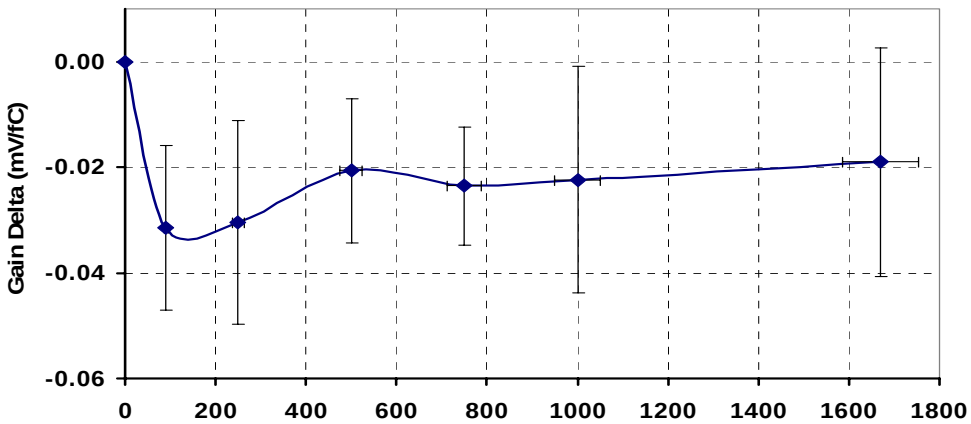



- Output DC Shift

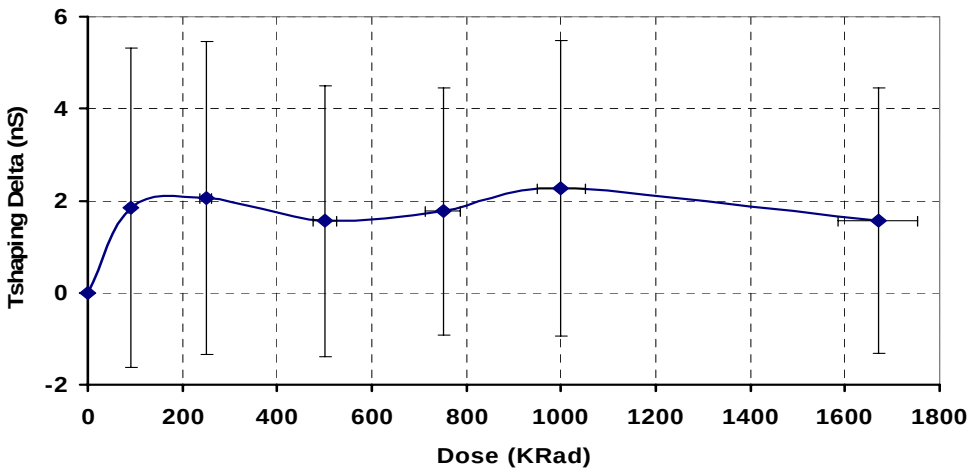



- Superimposed output waveform.
  - Preamp/Shaper is AC coupled in the system

# TID Test Results – Preamp/Shaper

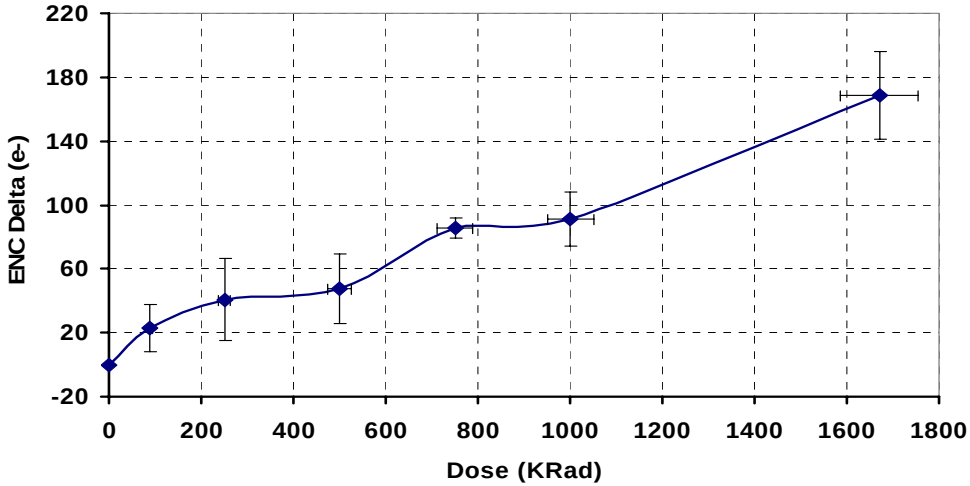



- Charge Gain

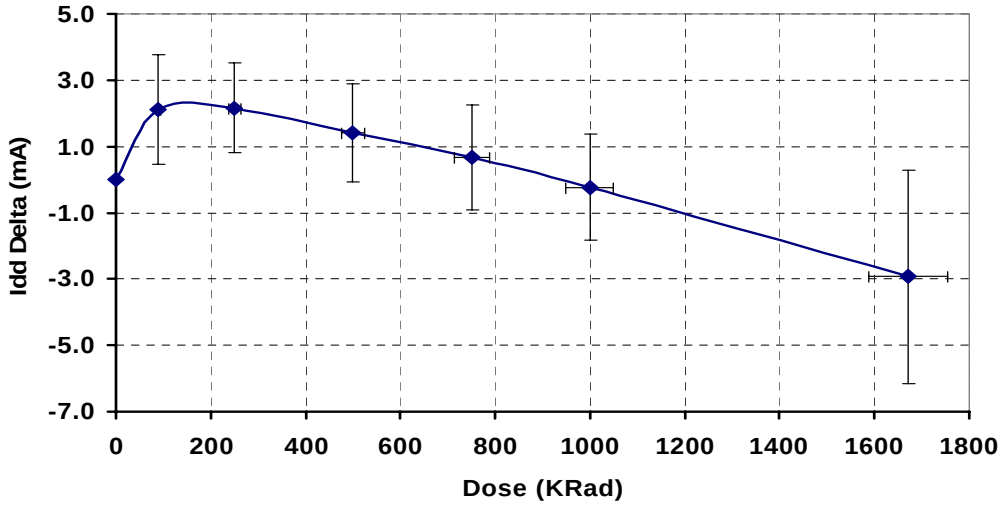



- Shaping Time

# TID Test Results – Preamp/Shaper

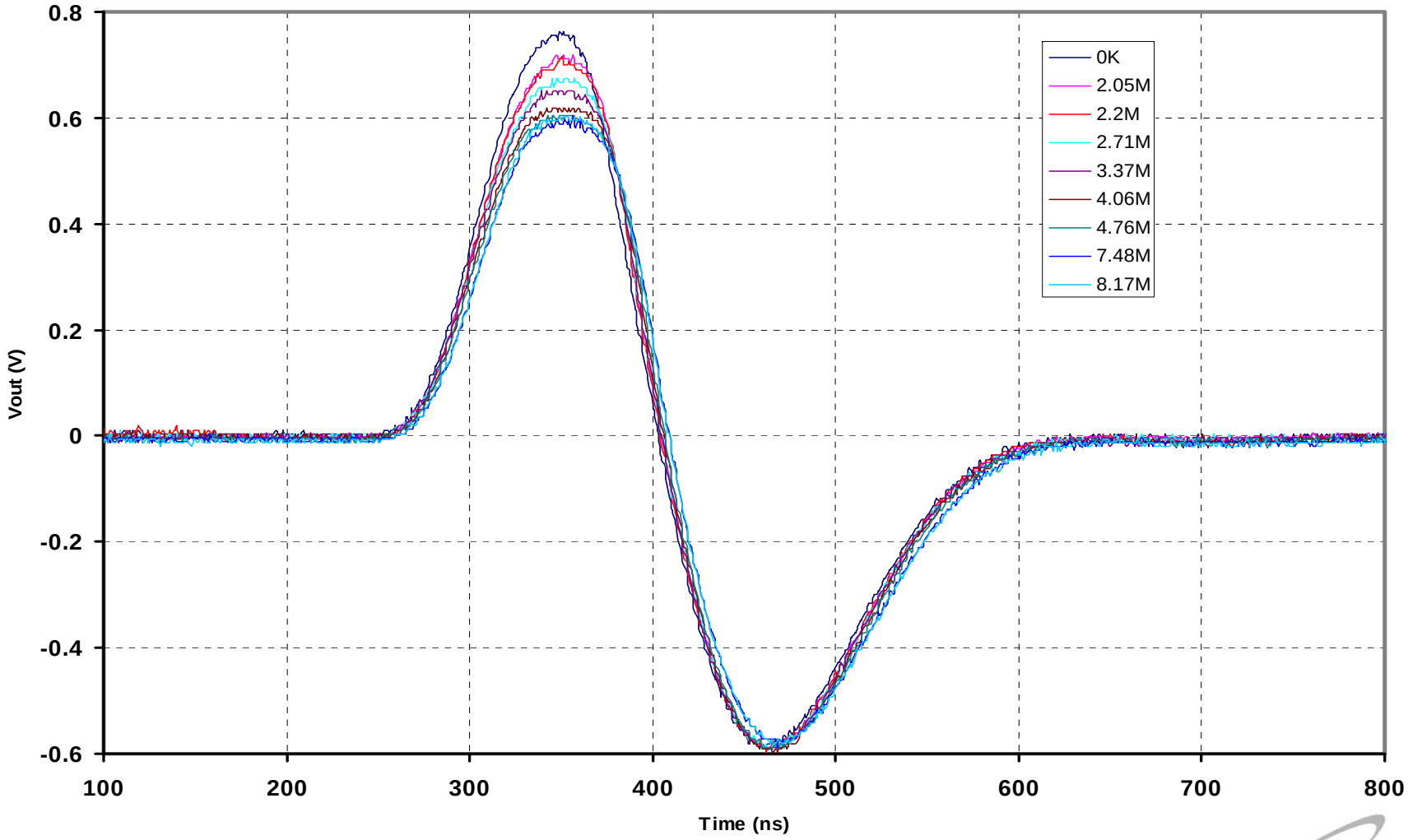



- ENC (r.m.s electrons)




- Device supply current

# IC71 TID extended beyond RTC



# IC71 NIEL Test Results

- 5 devices were irradiated using the PROSPERO reactor, France.
  - Total fluence achieved is $7.1 \times 10^{13}$ 1 MeV eq $n.cm^{-2}$

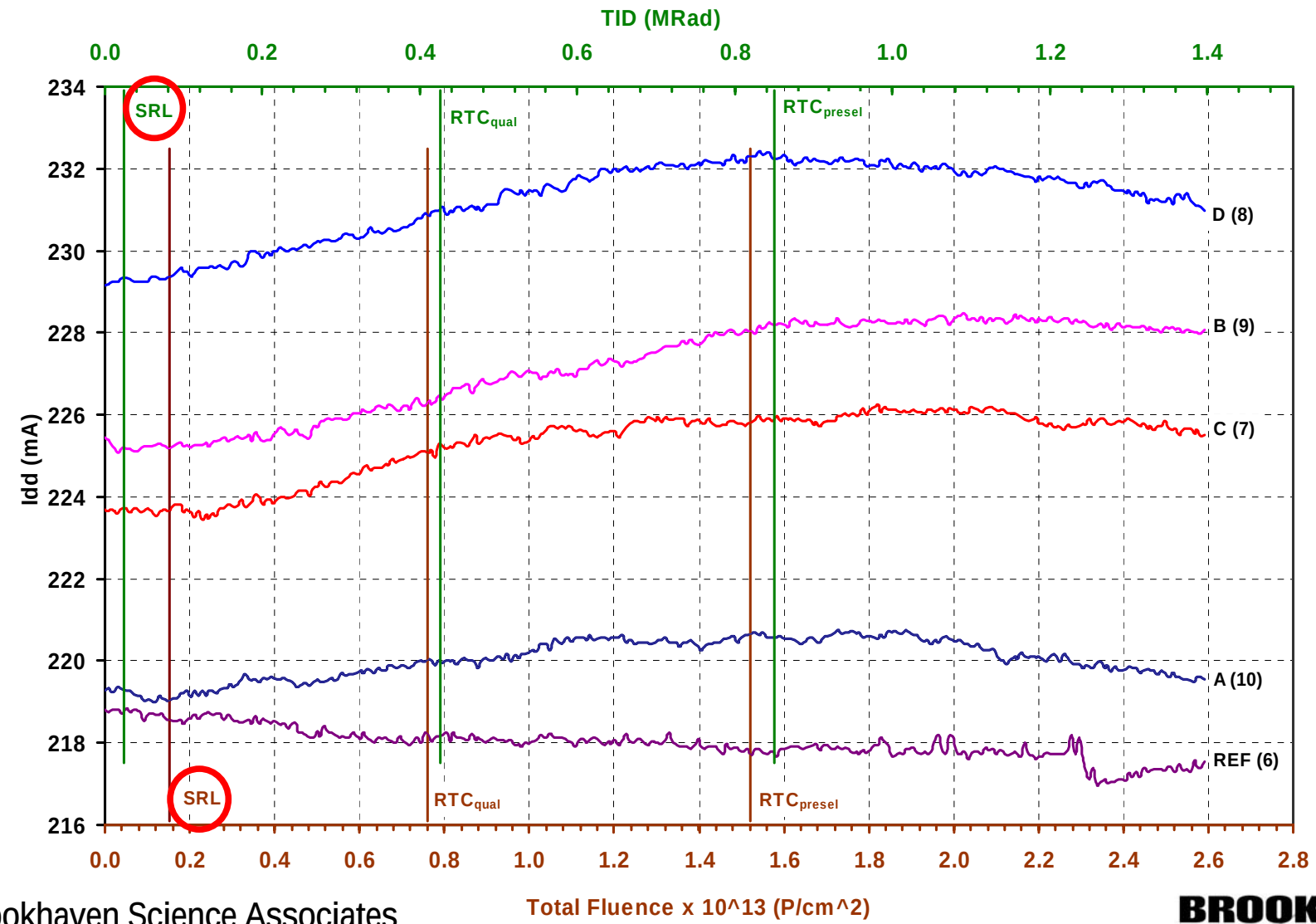
| Parameter | % Change from Pre-Radiation Measurement |
|---|---|
| Charge Gain | 1.5% |
| Shaping Time | 2.9% |
| ENC | 10.1% |
| Device Current | 2% |

# SEE/SEU Results - IC71

- Devices were irradiated with 226 MeV proton beam at the Mass. General NPTC facility to $2.54 \times 10^{13}$ p/cm$^2$
- Devices were monitored for Latch up during irradiation.
  - No Latch up or increase in device current were observed

| Parameter | % Change from Pre-Radiation Measurement |
|---|---|
| Charge Gain | 0.5% |
| Shaping Time | 0.8% |
| ENC | 12.9% |
| Device Current | 1.42% |

# IC71 supply current



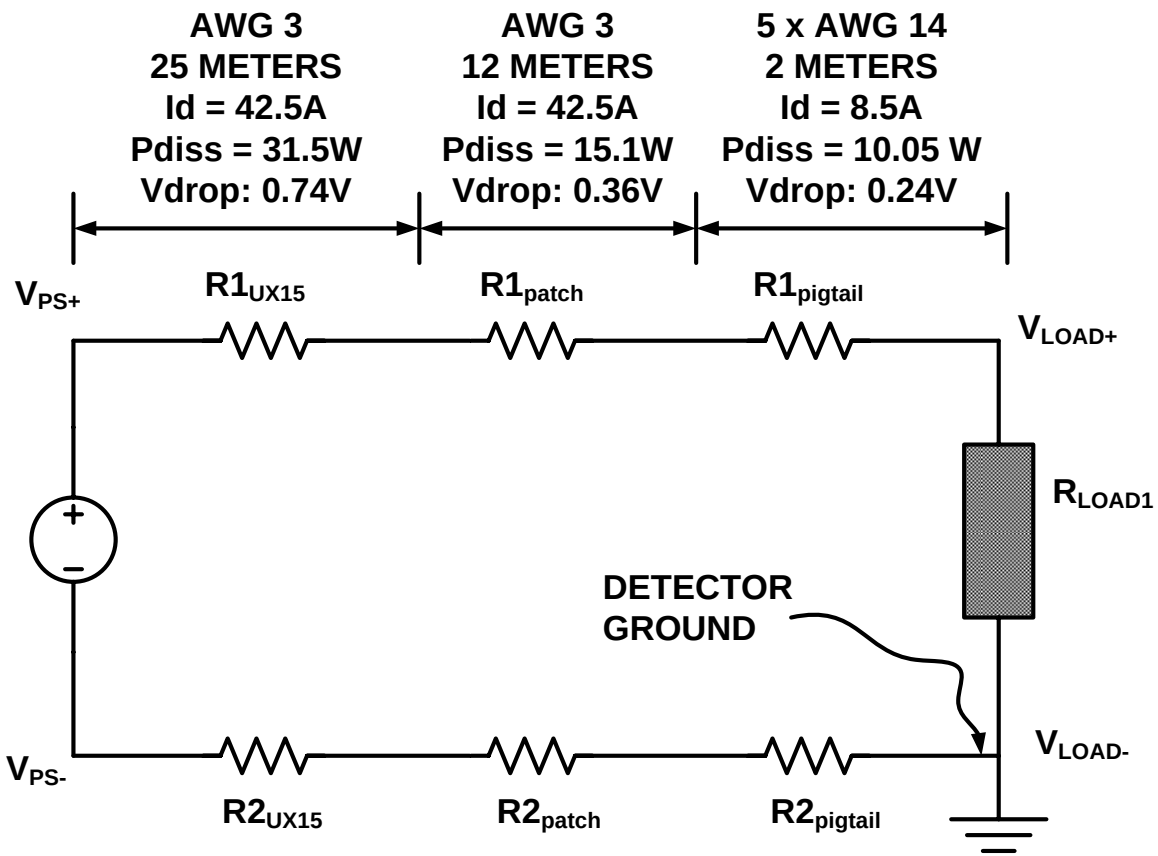
# Radiation Qualifications

- ASM1 Preamp Shaper ASIC has been tested for radiation dose effects.
  - well beyond the expected LHC levels
  - degradation are well within acceptable limits and functional
- L4913 LHC Regulators Qualified by CERN
- BAV99 Dual diodes have been Tested along with Preamp/Shaper ASIC.
- TVS for ESD has been tested/qualified by LAr

# Power and Grounding

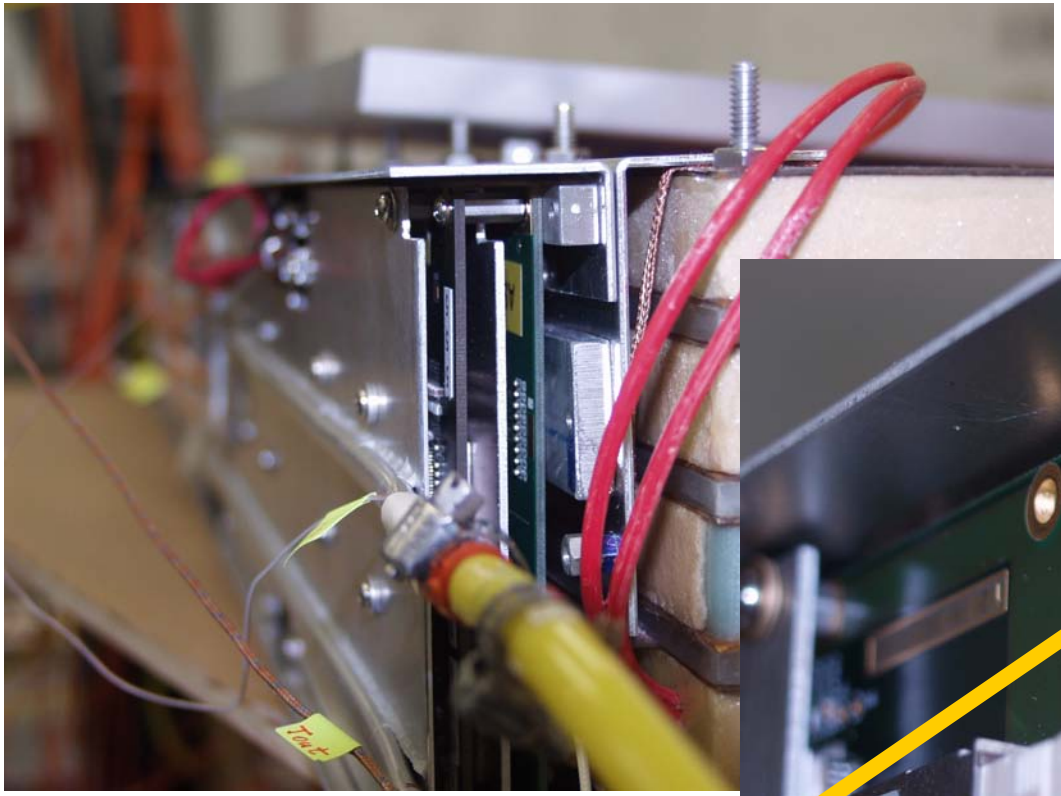
- ASM1 power is locally regulated to 3.3V from a 5V regulated source in ASM2.
- One connector is used for both power and signals
  - 32 Power pins
  - 64 GND pins
  - 100 signals + 4 N/C
- Power consumption $\approx$ 3.3V @ 0.950 A

# Power Supply & Distribution




- 5 Packs/Chamber
- 8.5A/Pack @ 7V
- Total Power
  13.6KW/endcap
  (3.6KW in cable)
- Each ASM pack will be fused in the patch panel

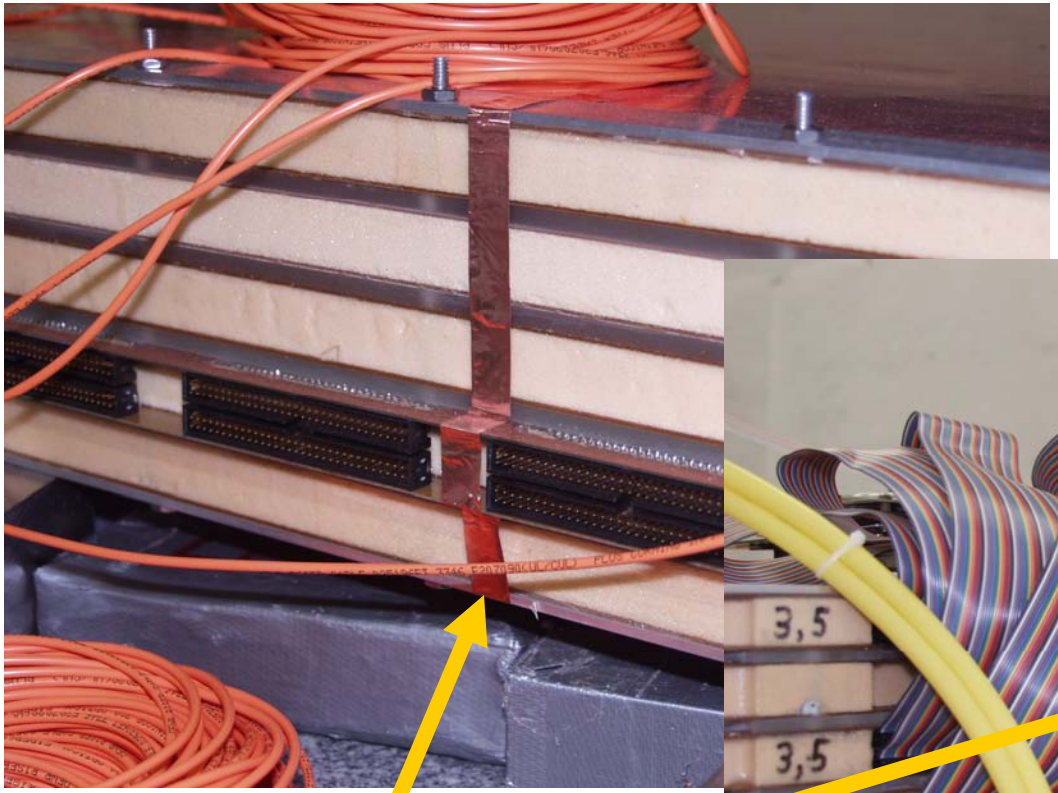
# Grounding



Faraday cage provides GND pickup for the ASM pack. Skin of the Chamber being “0”

GND pickup TABS in ASM1

# Additional Grounding Straps



straps are added to reinforce ground

# Production Plan/PCB Fabrication

- Upon approval, ASM1 to be fabricated to the following specs.
  - IPC-A-600
  - 6 mil line width/ 6 mil line spacing
  - Immersion Gold surface finish, 10u Au/100u Ni
- Boards will be Electrically tested to Gerber data
- Total 320 Boards + 10% spares
  - $ 26.57 / board for 350 boards in 8 weeks
- Fabricated boards will be shipped to BNL

# Production Plan/Assembly

- BNL will provide complete assembly kit for the vendor.
- Preamplifier/Shapers will be selected using the database and available lot statistics on circuit parameters.
- Vendor must be instructed to bake all Plastic packages to eliminate “pop corning”
  - Preamp/Shaper is packaged using MSL-1 material
  - LHC Regulator packaging material is not known

# Production Plan/Assembly

- Cost of Assembly per board: $ 59.98
- Assembler will do visual inspection of assembled boards.
- Initial shipment of Assembled boards:
  - Three weeks after task commencement
  - Eight weeks for completion

# Production Plan/Inspection & Testing

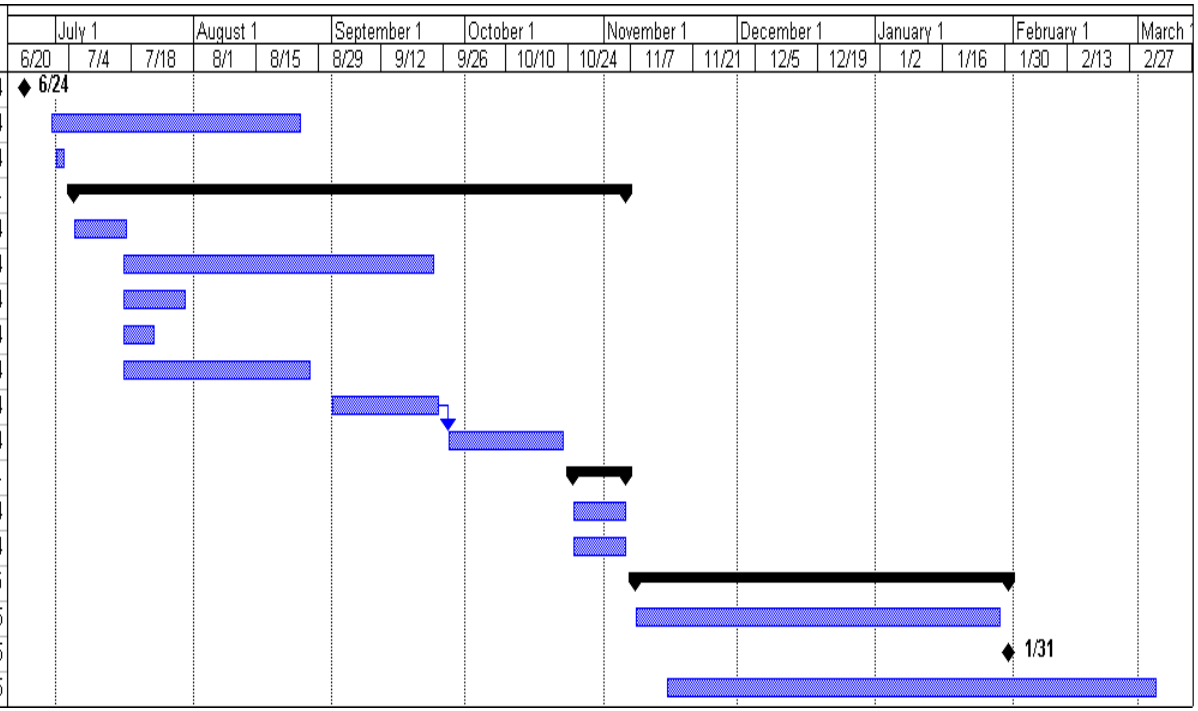
- Assembled boards will be shipped to BNL and visually inspected.
- Boards will be tagged with ATLAS standard barcode labels
- Any assembly failures will be either sent back to the assembler for correction or fixed internally based on the severity of the problem
- BNL's existing test fixtures will be used for electrically testing assembled ASM1 boards.

# Testing and Burn-in of ASM1

- A well characterized ASM2 will be used to test two ASM1 boards at a time with the aid of a signal injection board.
- Signal Injection board can either inject all 192 channels or combination of channels.
- Accepted ASM1 boards will be powered up for burn-in (168 hrs) and screened for failures before mounting on to the chamber.

# Items to be Procured for Production

| ITEM | Quanitity | Price | | Lead Time (weeks) |
|---|---|---|---|---|
| 0.1uF/25V Capacitor | 40,000 | $ | 680 | 0 |
| 1uF/16V Capacitor | 16,000 | $ | 320 | 0 |
| 10uF/25V Capacitor | 3000 | $ | 1,677 | 0 |
| 1.00K/1% 1/10W Resistor | 5000 | $ | 39 | 0 |
| 1.65K/1% 1/10W Resistor | 5000 | $ | 39 | 0 |
| 8.2/5% 1/10W Resistor | 70,000 | $ | 210 | 0 |
| 100K/1% 1/10W Resistor | 5000 | $ | 39 | 0 |
| 8.2/ESD Resistors | 33600 | $ | 29,904 | 10 |
| BAV99 Dual Diodes | 36000 | $ | 864 | 0 |
| Chamber connectors | 1500 | $ | 6,248 | 2 |
| ASM1 to ASM2 connectors | 350 | $ | 1,670 | 1 |
| ASM1 PCB Fabrication | 350 | $ | 10,350 | 8 |
| ASM1 Assembly | 350 | $ | 21,788 | 3 [8] |
| | | $ | 73,827 | |

# Production Timeline

| ID | | Task Name | Duration | Start | Finish |
|---|---|---|---|---|---|
| 1 | | CSC FrontEnd Board PRR | 0 days | Thu 6/24/04 | Thu 6/24/04 |
| 2 | | ASIC Testing | 8 wks | Wed 6/30/04 | Tue 8/24/04 |
| 3 | | New ASM1 Test | 2 days | Thu 7/1/04 | Fri 7/2/04 |
| 4 | | **Procurement** | **18 wks** | **Mon 7/5/04** | **Fri 11/5/04** |
| 5 | | Placing of Orders | 2 wks | Mon 7/5/04 | Fri 7/16/04 |
| 6 | | ESD Resistors | 10 wks | Fri 7/16/04 | Thu 9/23/04 |
| 7 | | Samtec Chamber Connectors | 2 wks | Fri 7/16/04 | Thu 7/29/04 |
| 8 | | ASM1/ASM2 Connectors | 1 wk | Fri 7/16/04 | Thu 7/22/04 |
| 9 | | ASM1 Fabrication | 6 wks | Fri 7/16/04 | Thu 8/26/04 |
| 10 | | Assembly Kit Preparation | 3.6 wks | Wed 9/1/04 | Fri 9/24/04 |
| 11 | | ASM1 Assembly | 4 wks | Mon 9/27/04 | Fri 10/22/04 |
| 12 | | **Production End** | **2 wks** | **Mon 10/25/04** | **Fri 11/5/04** |
| 13 | | Inspection & Test | 2 wks | Mon 10/25/04 | Fri 11/5/04 |
| 14 | | Board Rework | 2 wks | Mon 10/25/04 | Fri 11/5/04 |
| 15 | | **Assembly and Burn in** | **12 wks** | **Mon 11/8/04** | **Mon 1/31/05** |
| 16 | | Burn in (30 ASM1/ week) | 12 wks | Mon 11/8/04 | Fri 1/28/05 |
| 17 | | CSC ASM1 Production Complete | 0 wks | Mon 1/31/05 | Mon 1/31/05 |
| 18 | | Electronics & Chamber Integration | 16 wks | Mon 11/15/04 | Fri 3/4/05 |