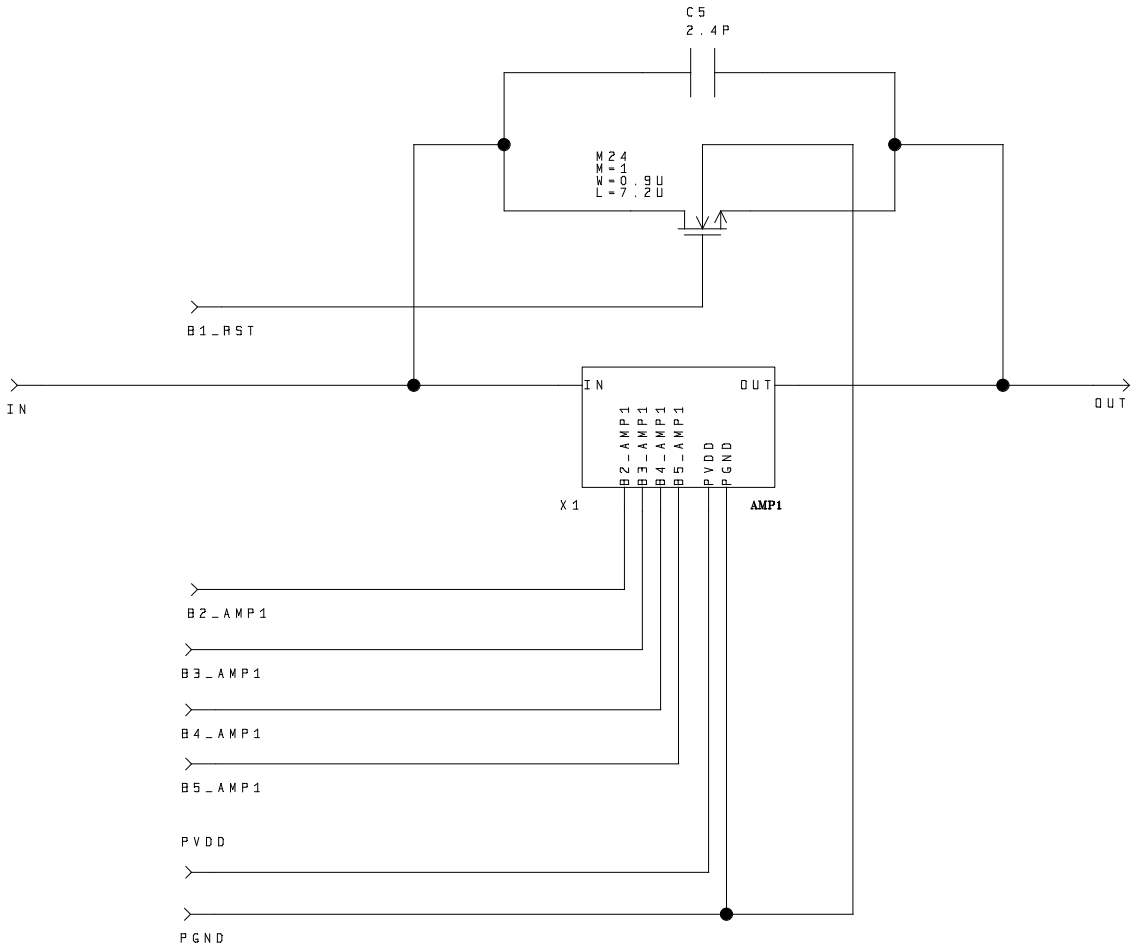

Bias lines:

- B1_RST
- B2_AMP1
- B3_AMP1
- B4_AMP1 **
- B5_AMP1

PVDD: 3.3V
PGND: 0V
Rf: 1M
Pdiss: 15mW

Notes:

** BIAS line B4_AMP1 is grounded ** off chip

@DATETIME=5-31-2001_13:34
@SHEET=1

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Approvals	Date	Drawing: ATLAS CSC / HP CMOS14TB 0.5U PREAMP
Drawn		
Checked		
Issued		
SIZE	B	IC71
DWG NO:		
REV NO:	1	
SCALE		Sheet: 1 of 1

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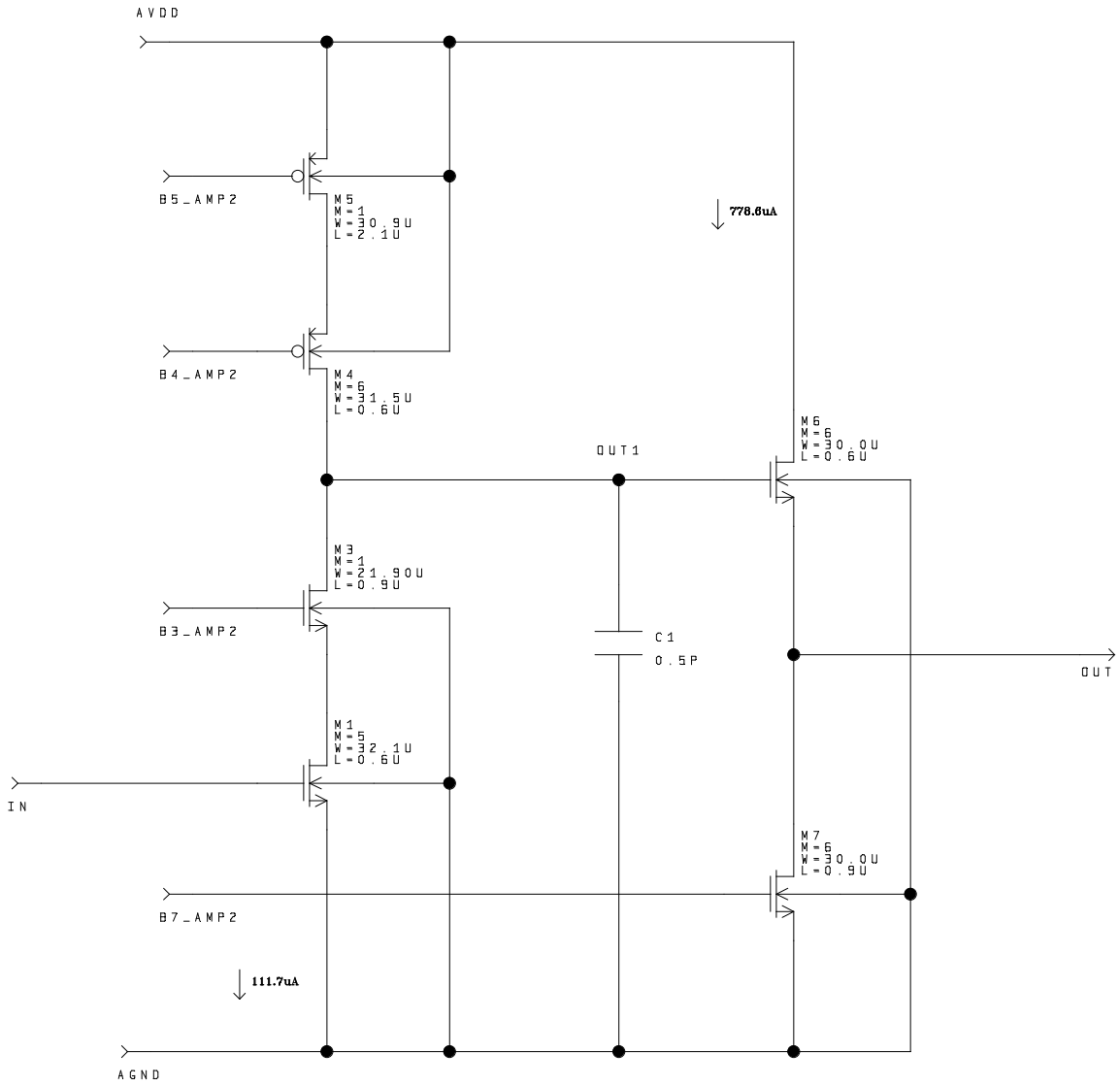

Bias lines:

B3_AMP2
B4_AMP2
B5_AMP2
B7_AMP2

AVDD: 3.3V
AGND: 0V

Pdiss: 2.9mW

Notes:

Changed the Following:

M1 W=32U to W=32.1U
M3 W=22U to 21.9U
M5 W=31U to 30.9U

@DATETIME=5-26-1999_12:54
@SHEET=1

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Drawing:

ATLAS CSC / HP CMOS14TB 0.5U
AMP2

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

IC71

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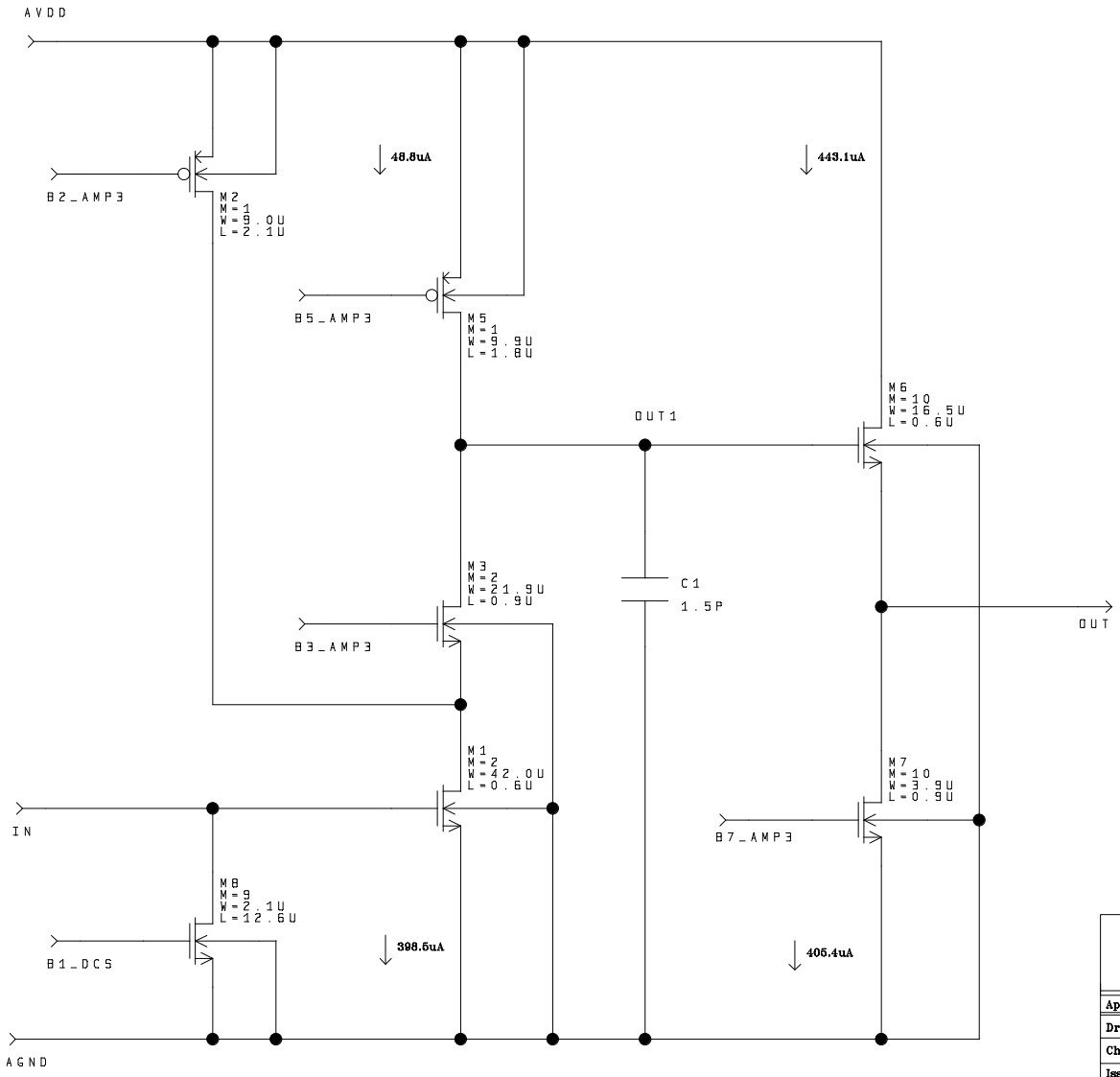
Sheet: 1 of 1



Bias lines:

B1_DCS
B2_AMP3
B3_AMP3
B5_AMP3
B7_AMP3

AVDD: 3.3V
AGND: 0V

Pdiss: 2.6mW

Notes:

Changed the Following:

M3 W=9.1U to 9.0U
M3 W=22U to 21.9U
M4 W=16.4U to 16.5U
M4 W=9.8U to 9.9U

@DATETIME=5-26-1999_13:03
@SHEET=1

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Approvals	Date	Drawing: ATLAS CSC / HP CMOS14TB 0.5U AMP3
Drawn		
Checked		
Issued		
SIZE	B	IC71
DWG NO:		
REV NO:	1	
SCALE		

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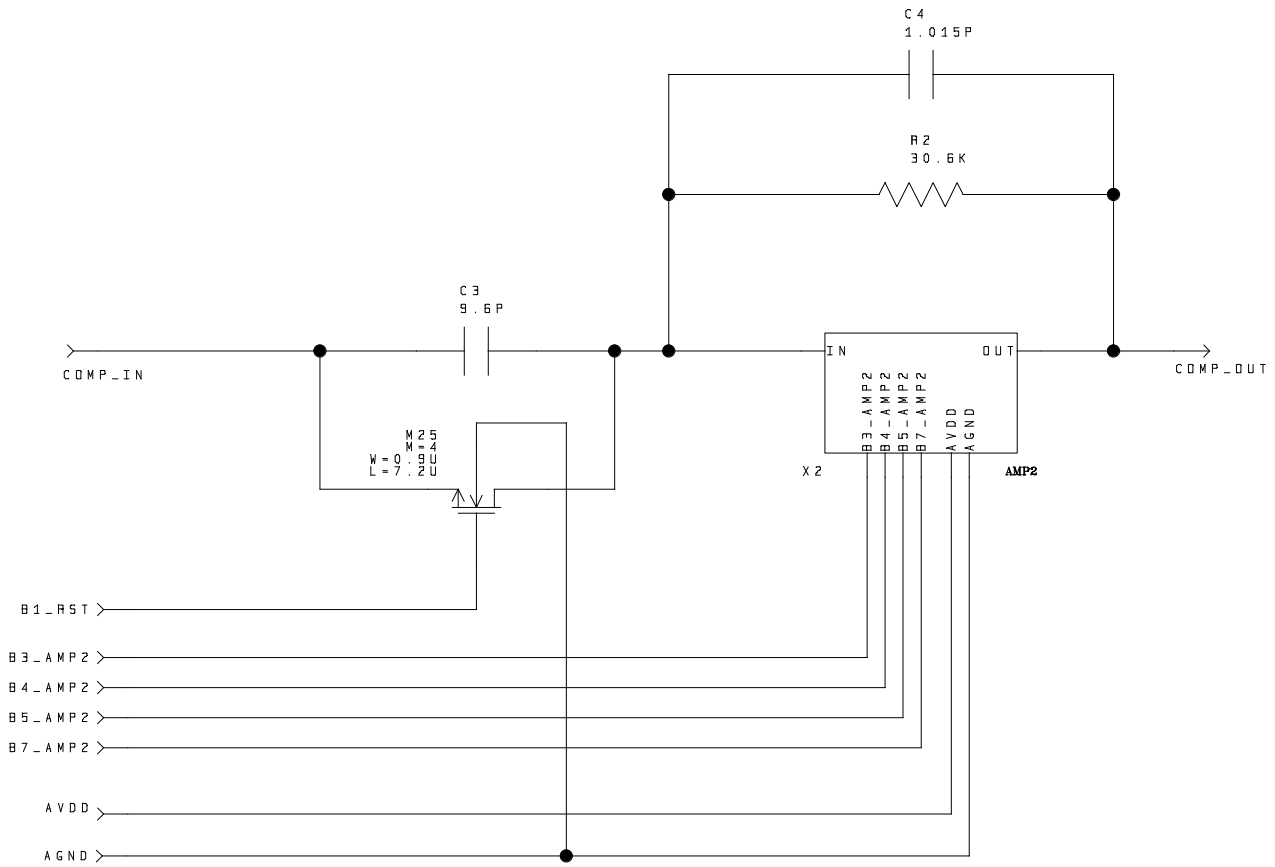
Sheet: 1 of 1



Bias lines:

B1_RST
B3_AMP2
B4_AMP2
B5_AMP2
B7_AMP2

AVDD: 3.3V
AGND: 0V

Notes:

M25 : Four copied of M24 (Feedback FET of PREAMP) – Layout

@DATETIME=6-7-2001_12:22
@SHEET=1

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Approvals	Date	Drawing: ATLAS CSC / HP CMOS14TB 0.5U COMPENSATION
Drawn		
Checked		
Issued		
SIZE	B	IC71
DWG NO:		
REV NO:	1	
SCALE		

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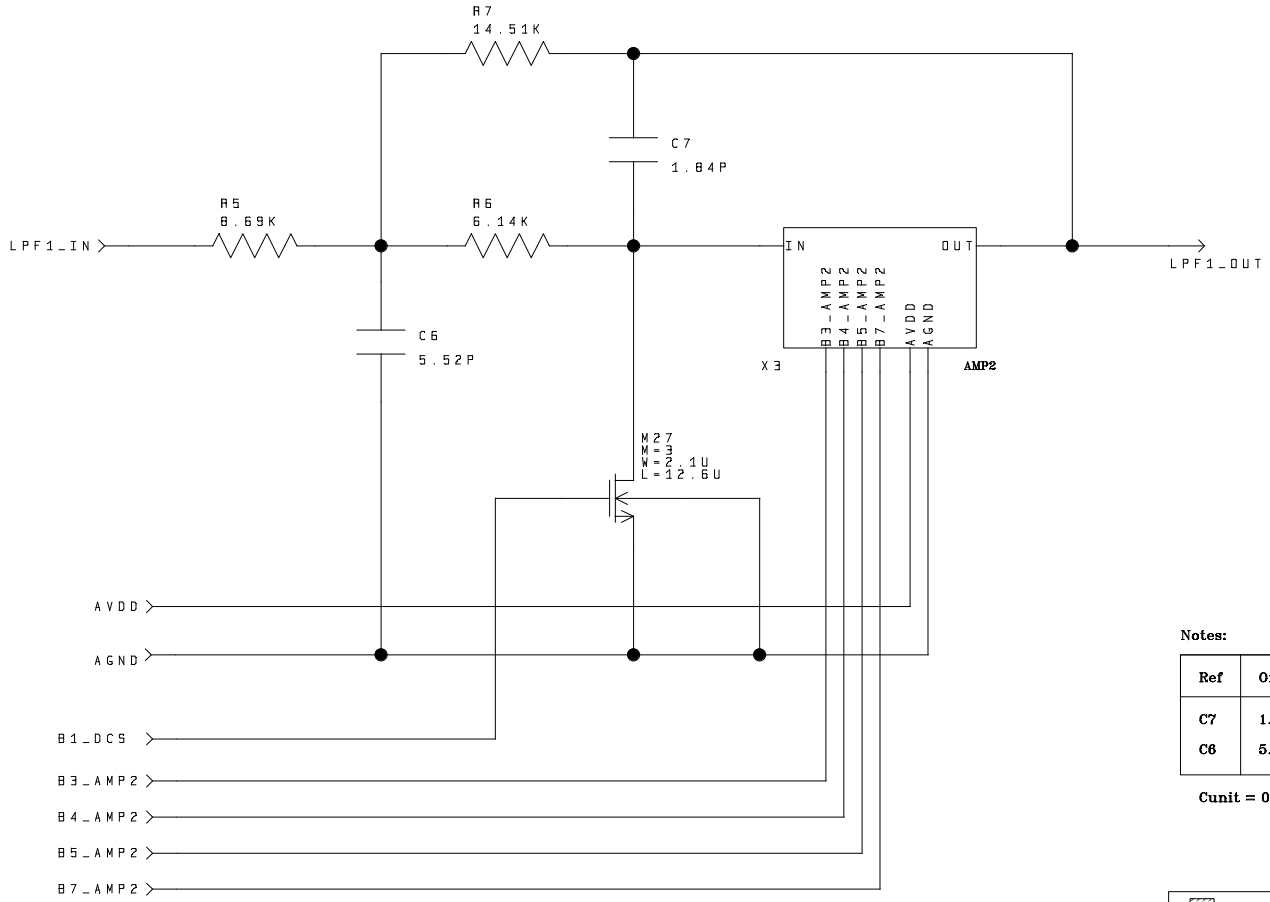
Sheet: 1 of 1

SEE NOTES ON THESE VALUES



Bias lines:

B3_AMP2
B4_AMP2
B5_AMP2
B7_AMP2
B1_DCS

AVDD: 3.3V
AGND: 0V

Notes:

Ref	Original	Changed	Copies	Error	Ratio
C7	1.88P	1.84P	Cunit*2	–	–
C6	5.52P	5.52P	Cunit*6	2.2%	C6/C7 = 2.936

Cunit = 0.92P

@DATETIME=5-26-1999_15:08
@SHEET=1

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Approvals	Date
Drawn	
Checked	
Issued	

Drawing:

ATLAS CSC / HP CMOS14TB 0.5U
Low Pass Filter Stage 1

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

IC71

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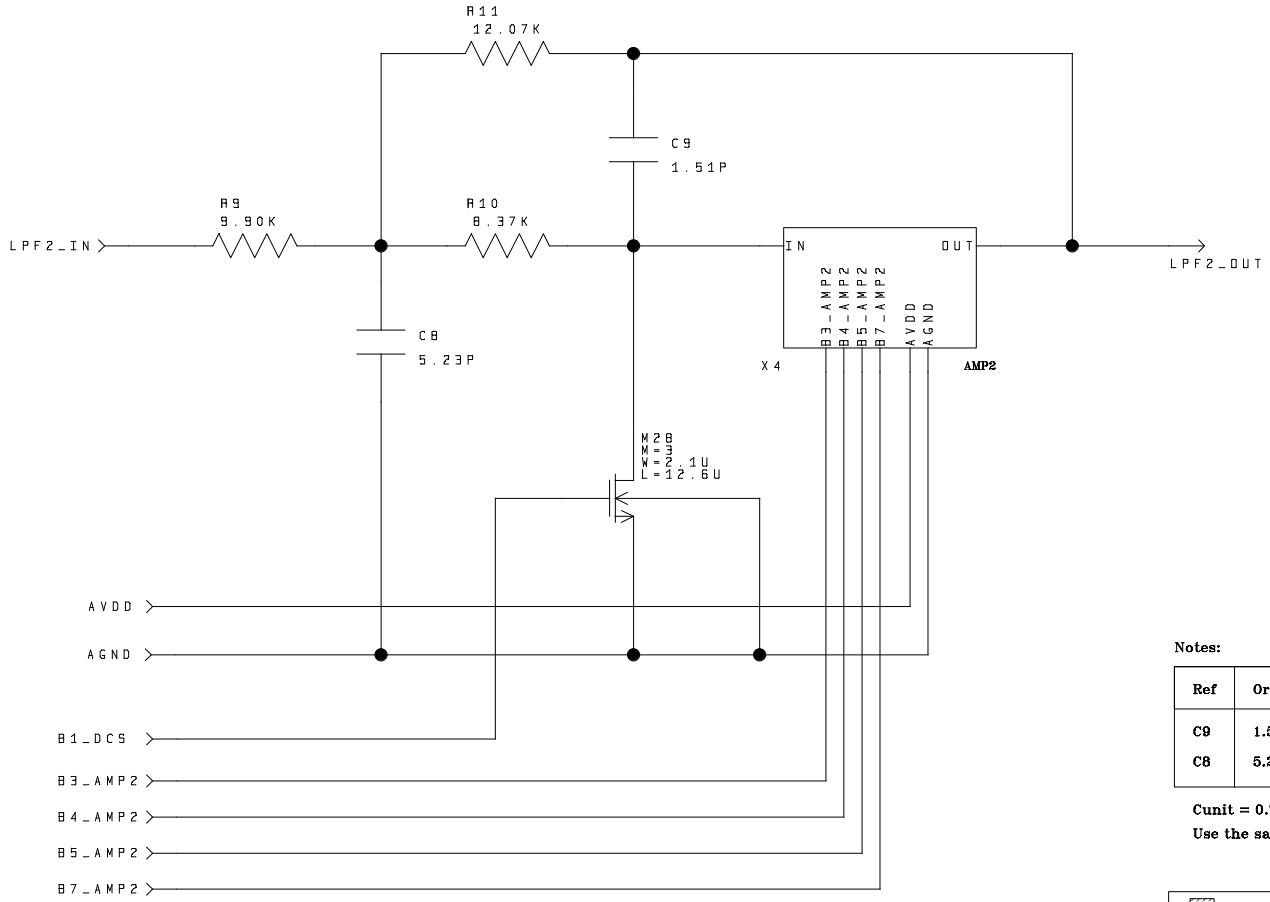
SEE NOTES ON THESE VALUES



Bias lines:

B3_AMP2
B4_AMP2
B5_AMP2
B7_AMP2
B1_DCS

AVDD: 3.3V
AGND: 0V

Notes:

Ref	Original	Changed	Copies	Error	Ratio
C9	1.51P	1.5P	Cunit*2	–	–
C8	5.23P	5.25P	Cunit*7	1%	C8/C9 = 3.463

Cunit = 0.75P

Use the same Unit Capacitance in BP stage also

@DATETIME=5-26-1999_15:08
@SHEET=1

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Approvals	Date
Drawn	
Checked	
Issued	

Drawing:

ATLAS CSC / HP CMOS14TB 0.5U
Low Pass Filter Stage 2

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

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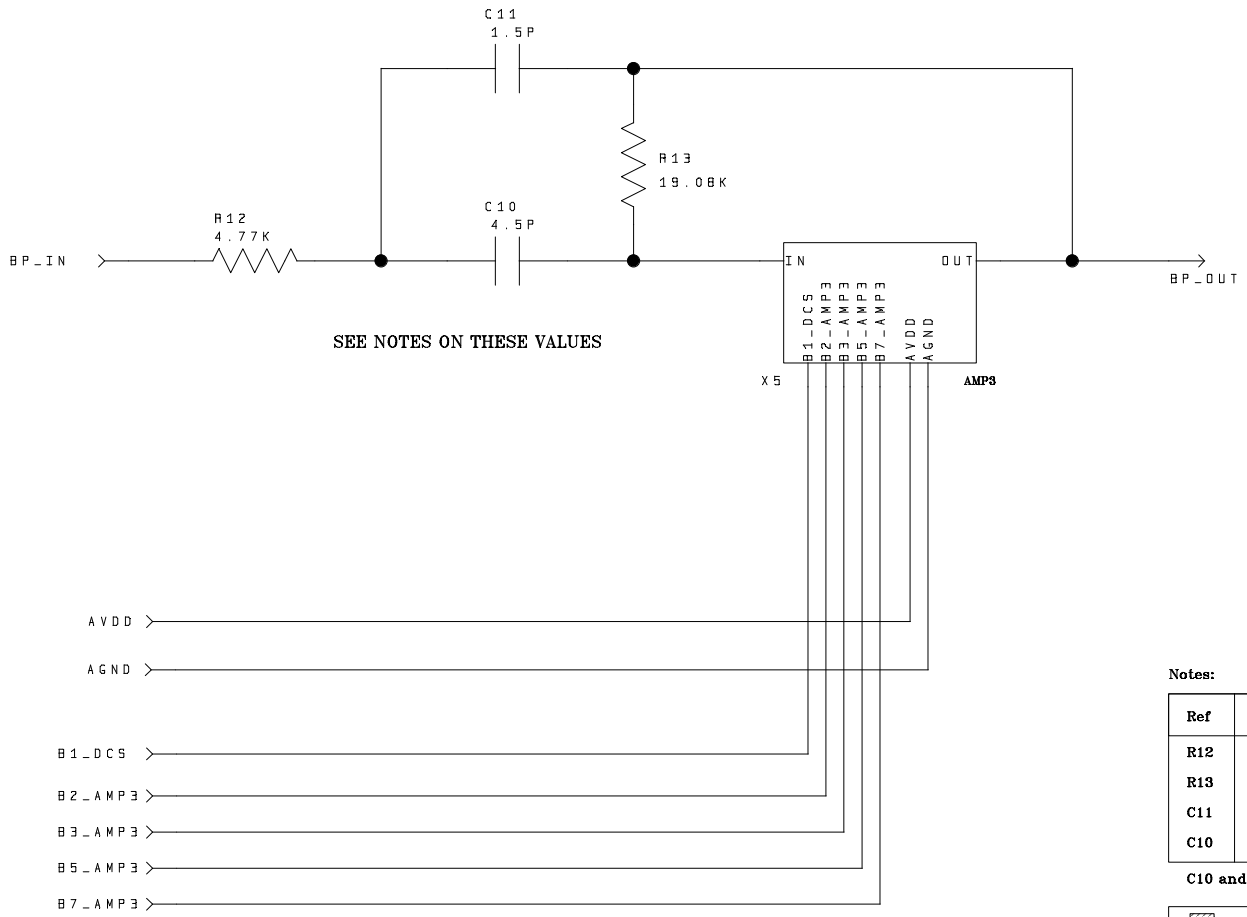
Sheet: 1 of 1



Bias lines:

B2_AMP3
B3_AMP3
B5_AMP3
B7_AMP3
B1_DCS

AVDD: 3.3V
AGND: 0V

Notes:

Ref	Original	Changed	Copies	Error	Ratio
R12	4.77K	4.77K	R12*1	–	–
R13	18.93K	19.08K	R12*4	0.8%	R13/R12 = 3.968
C11	1.46P	1.5P	C11*1	–	–
C10	4.53P	4.5P	C11*3	3.4%	C10/C11 = 3.102

C10 and C11 : Use Unit capacitance of 0.75P used in LP2 C9 and C8

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Drawing:

ATLAS CSC / HP CMOS14TB 0.5U
Band Pass Filter

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

IC71

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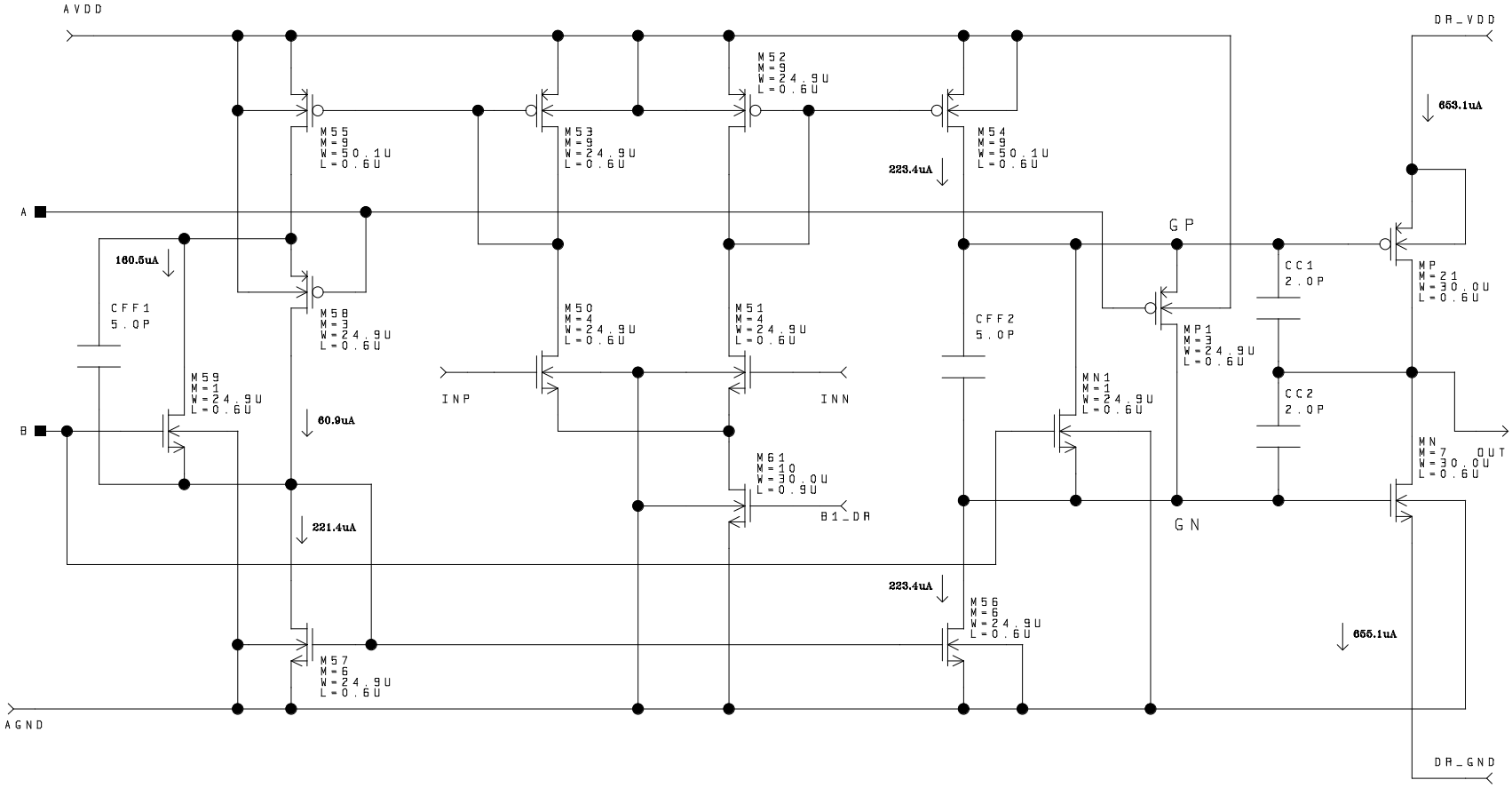
@DATETIME=5-26-1999_15:09
@SHEET=1



Notes:

Changed the Following:
M50,M51,M52,M53,M56,M57,M58,M59,MP1 and MN1 W=25U to 24.9U
M54 and M55 W=50U to 50.1U

Bias lines:
A
B
B1_DR
B2_DR

AVDD/DR_VDD: 3.3V
GND/DR_GND: 0V

Pdiss: 4.5mW

@DATETIME=5-26-1999_13:10
@SHEET=1

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Approvals	Date
Drawn	
Checked	
Issued	
SIZE	B
DWG NO:	
REV NO:	1
SCALE	

Drawing:
ATLAS CSC / HP CMOS14TB 0.5U
CLASS AB DRIVER

IC71

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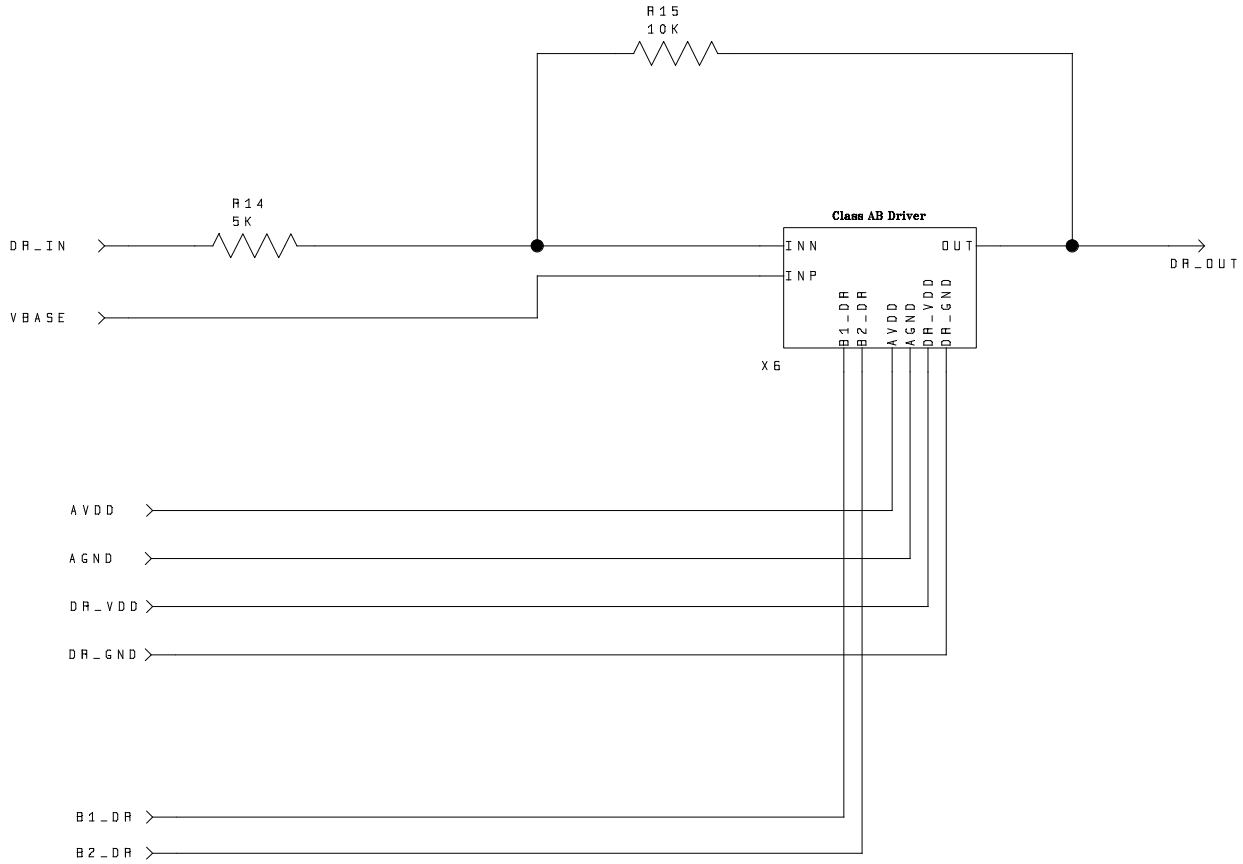
Sheet: 1 of 2



Bias lines:
A
B
B1_DR
B2_DR

AVDD/DR_VDD: 3.3V
AGND/DR_GND: 0V

Notes:
R15 = Two R14's in Series (Layout)

@DATETIME=5-26-1999_15:10
@SHEET=1

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Approvals	Date	Drawing:
Drawn		ATLAS CSC / HP CMOS14TB 0.5U OUTPUT DRIVE STAGE
Checked		
Issued		
SIZE	B	IC71
DWG NO:		
REV NO:	1	
SCALE		

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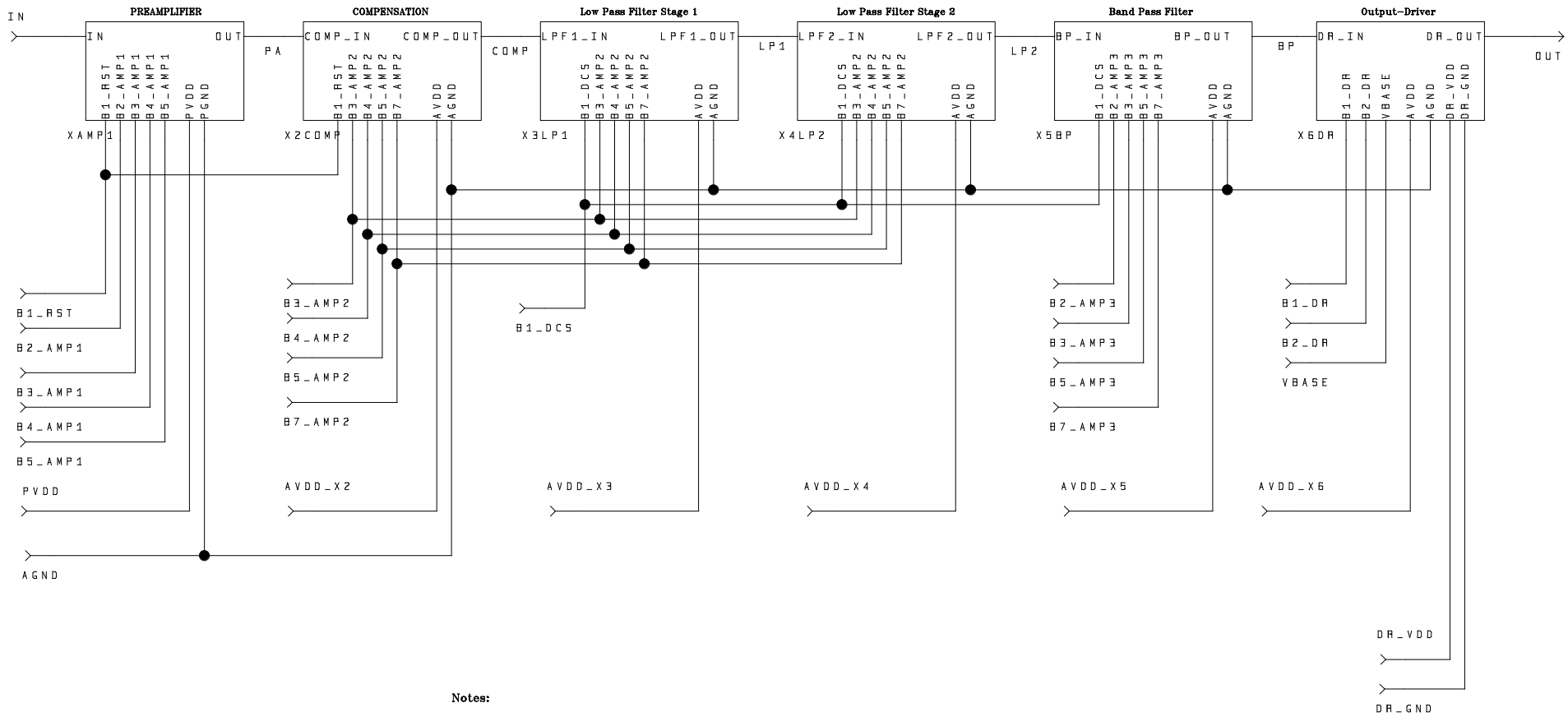

Notes:

PVDD: 3.3V
AVDD: 3.3V
DR_VDD: 3.3V
PGND: 0V
DR_GND: 0V

@DATETIME=6-7-2001_12:22
@SHEET=1

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Approvals	Date
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Drawing:

ATLAS CSC / HP CMOS14TB 0.5U
CSC Preamp/Shaper Channel

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

IC71

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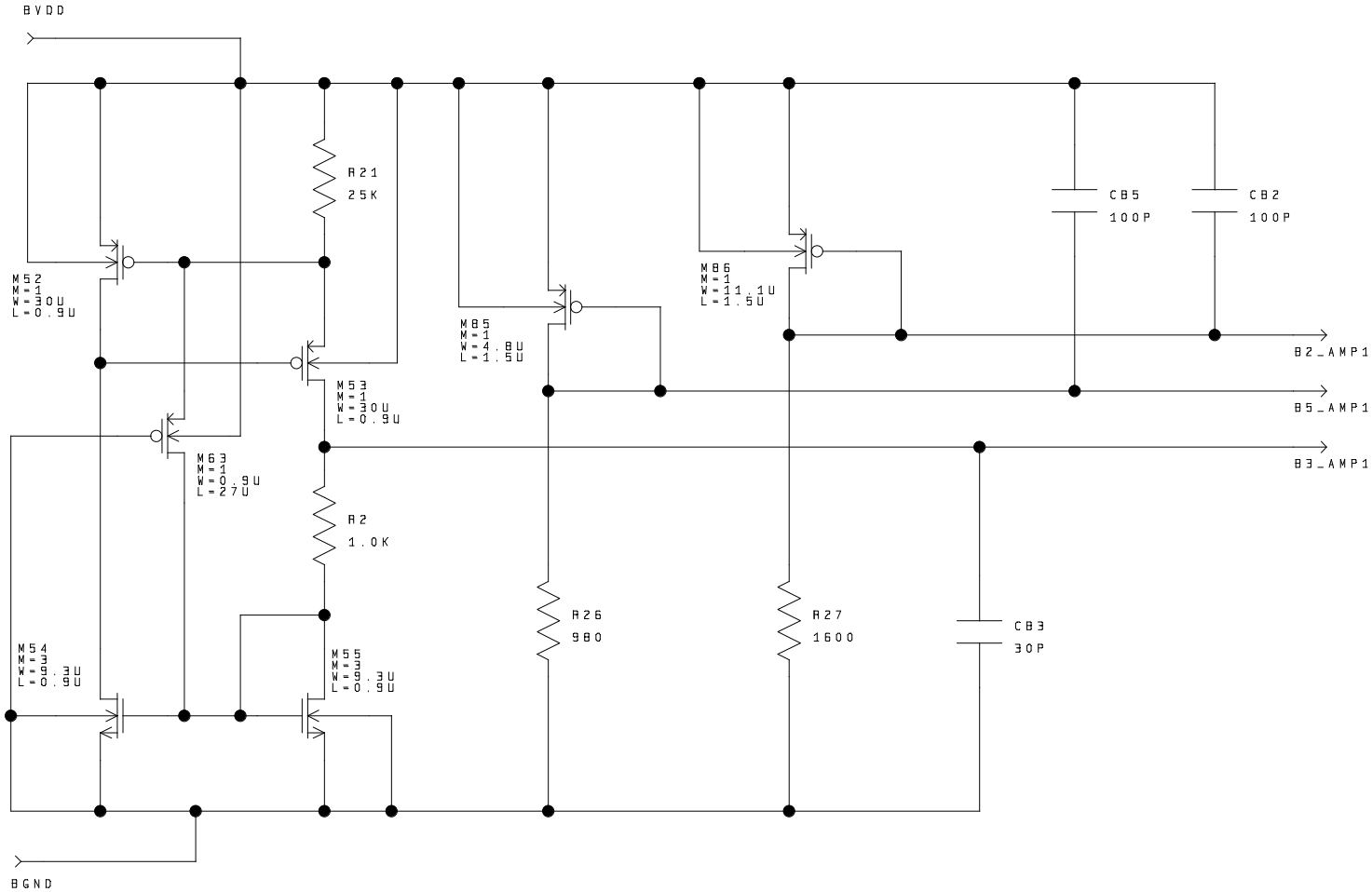

Notes:

Changed the Following:

M86 and M81 W=11.2U to 11.1U
M83 and M55 W=52.01U to 51.9U

B4_AMP1 NODE is GROUNDED at the AMP1 LEVEL

Bias lines:

B1_RST
B2_AMP1
B3_AMP1
B4_AMP1 ** is grounded at AMP1 level
B5_AMP1

BVDD: 3.3V
BGND: 0V

@DATETIME=5-26-1999_13:56
@SHEET=1

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Approvals	Date
Drawn	
Checked	
Issued	

Drawing:

ATLAS CSC / HP CMOS14TB 0.5U
AMP1 and RESET BIAS

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

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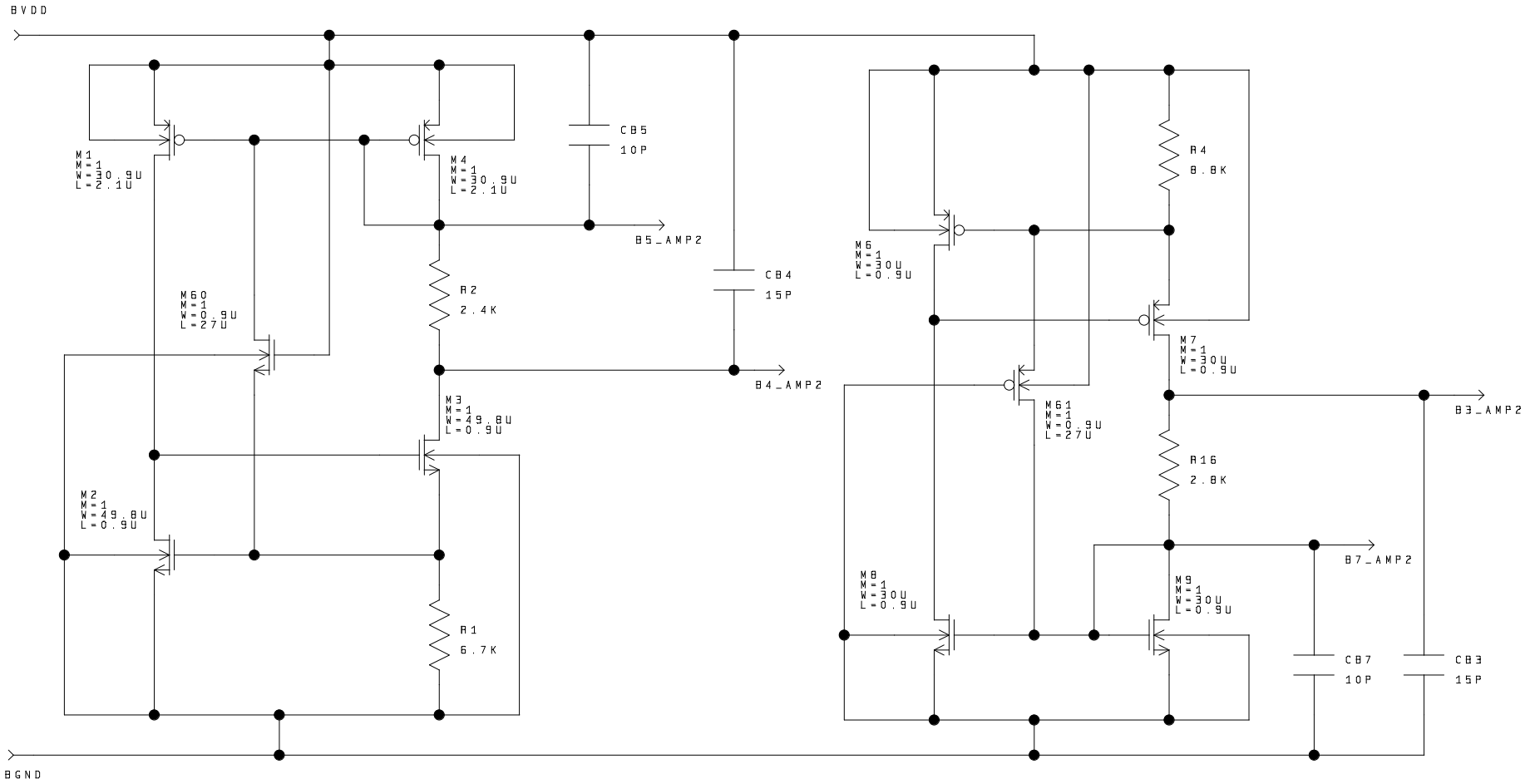

Notes:

Changed the Following:

M1 and M4 W=31U to 30.9U

Bias lines:

B3_AMP2
B4_AMP2
B5_AMP2
B7_AMP2

BVDD: 3.3V
BGND: 0V

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Approvals	**Date**	**Drawing:** ATLAS CSC / HP CMOS14TB 0.5U AMP2-BIAS
Drawn		
Checked		
Issued		
SIZE	**B**	IC71
DWG NO:		
REV NO:	**1**	
SCALE		

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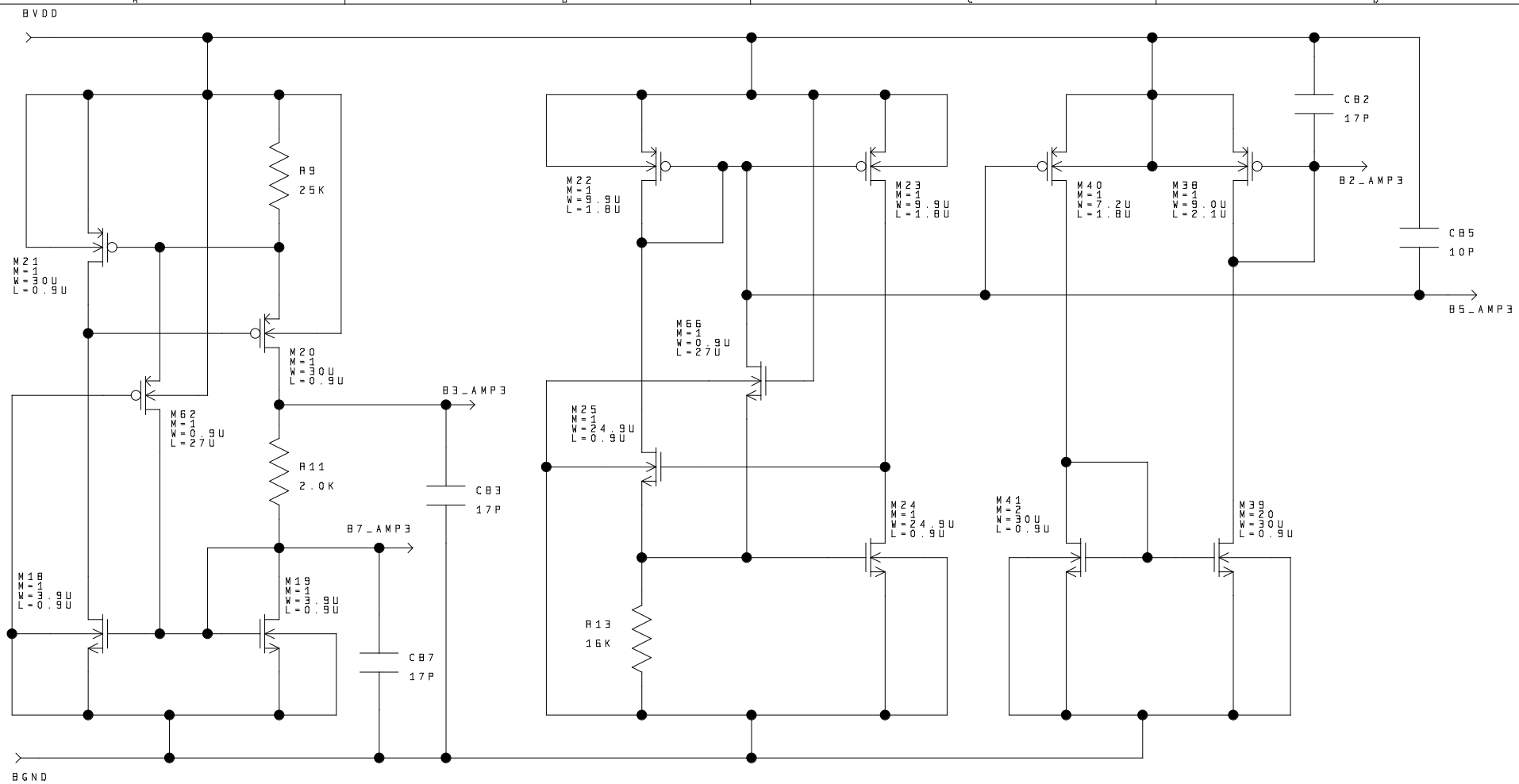
Sheet: 1 of 1

@DATETIME=5-26-1999_14:07
@SHEET=1



Notes:

Changed the Following:

M22 and M23 W=9.8U to 9.9U
M24 and M25 W=25U to 24.9U
M38 W=9.1U to 9.0U

Bias lines:

B2_AMP3
B3_AMP3
B5_AMP3
B7_AMP3

BVDD: 3.3V
BGND: 0V

@DATETIME=5-26-1999_14:20
@SHEET=1

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Approvals	Date	Drawing:
Drawn		ATLAS CSC / HP CMOS14TB 0.5U AMP3-BIAS
Checked		
Issued		
SIZE	B	IC71
DWG NO:		
REV NO:	1	
SCALE		

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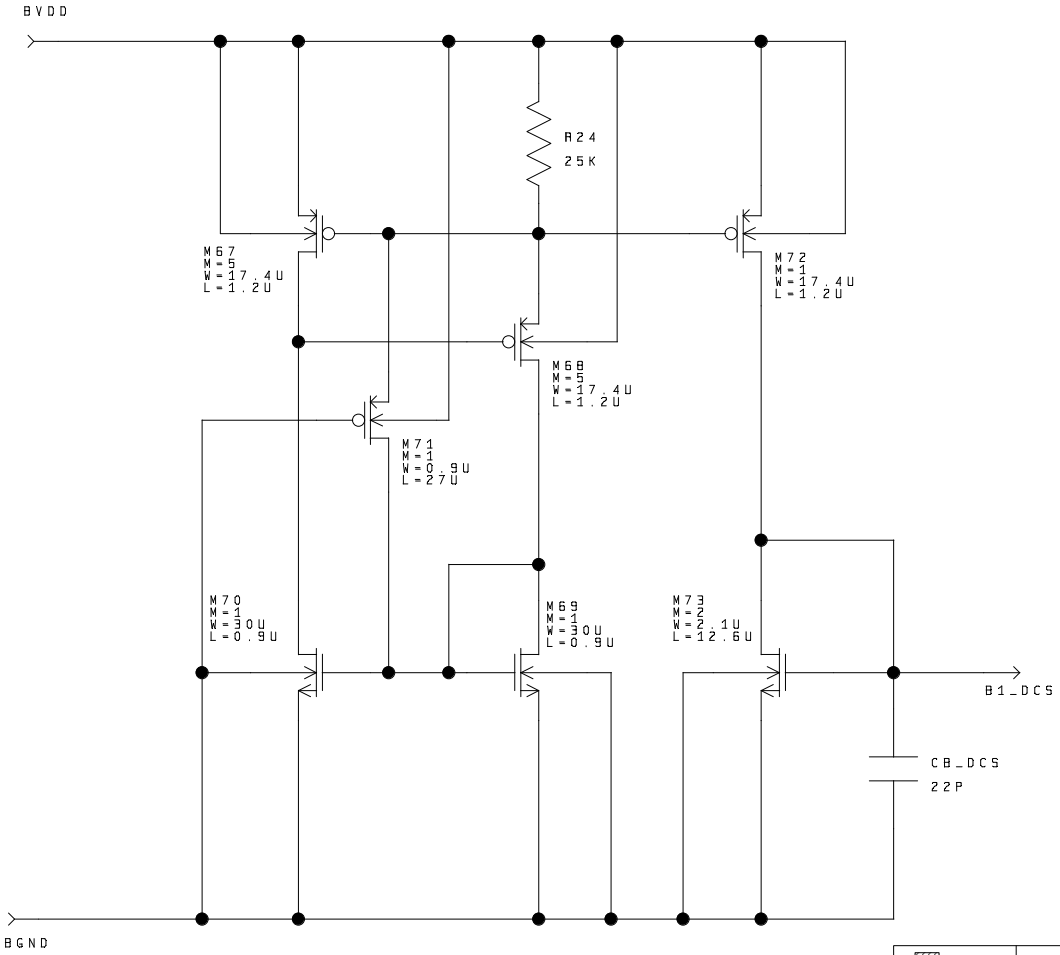
Bias lines:
B1_DCS

BVDD: 3.3V
BGND: 0V



Notes:

@DATETIME=5-26-1999_14:27
@SHEET=1

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Approvals	Date	Drawing:
Drawn		ATLAS CSC / HP CMOS14TB 0.5U DC Control Bias
Checked		
Issued		
SIZE	B	IC71
DWG NO:		
REV NO:	1	
SCALE		

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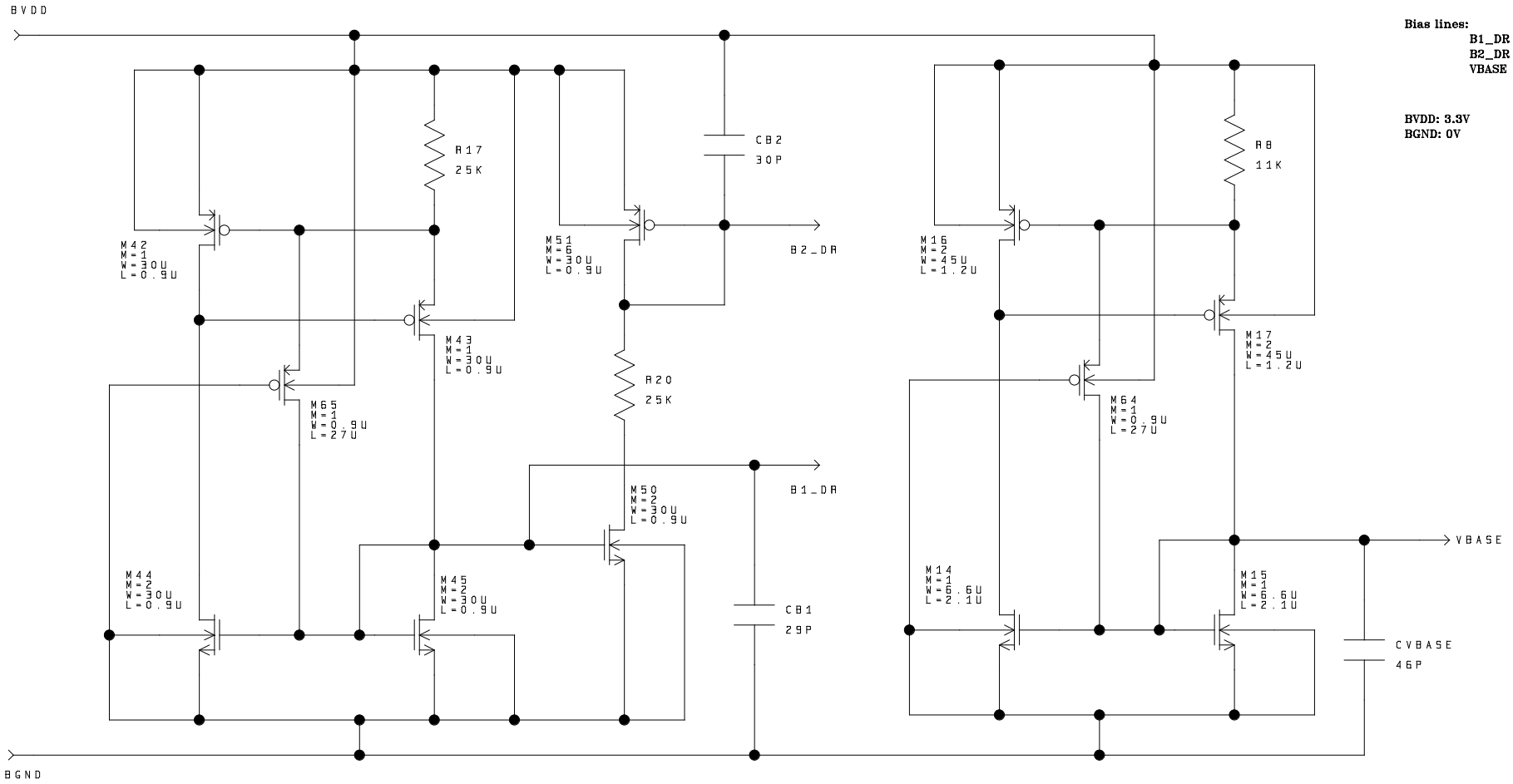

Bias lines:

B1_DR
B2_DR
VBASE

BVDD: 3.3V
BGND: 0V

Notes:

Changed the following:

M67 and M17 : M=1,W=90U to M=2,W=45U

@DATETIME=5-26-1999_14:36
@SHEET=1

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Approvals	Date	Drawing:
Drawn		ATLAS CSC / HP CMOS14TB 0.5U CLASS AB DRIVER-BIAS
Checked		
Issued		
SIZE	B	IC71
DWG NO:		
REV NO:	1	
SCALE		

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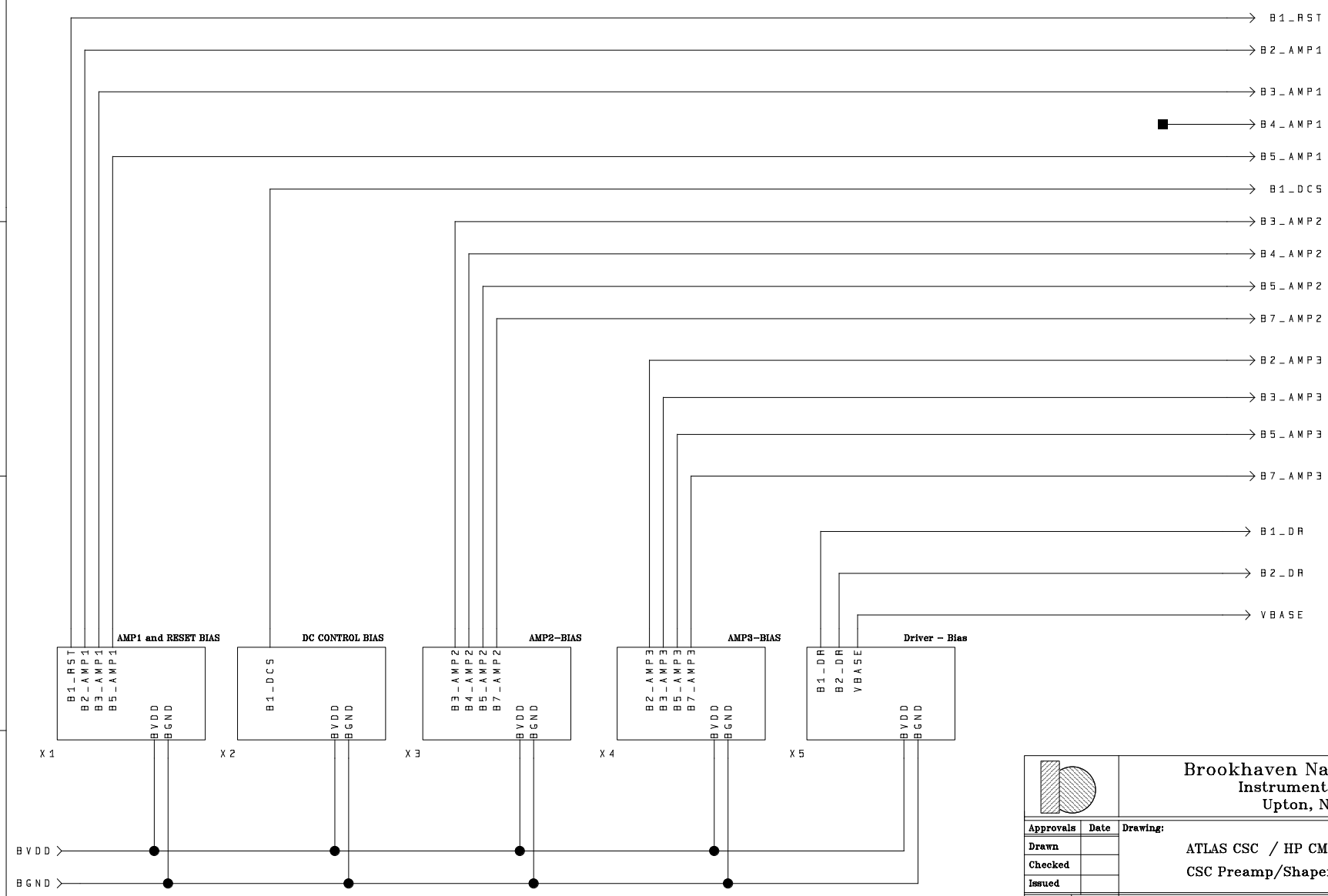
Sheet: 1 of 1



Notes:

BVDD: 3.3V
BVDD: 3.3V

@DATETIME=5-26-1999_17:43
@SHEET=1

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Approvals	Date
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Drawing:

ATLAS CSC / HP CMOS14TB 0.5U
CSC Preamp/Shaper/Driver BIAS

SIZE	B
DWG NO:	
REV NO:	1
SCALE	

IC71

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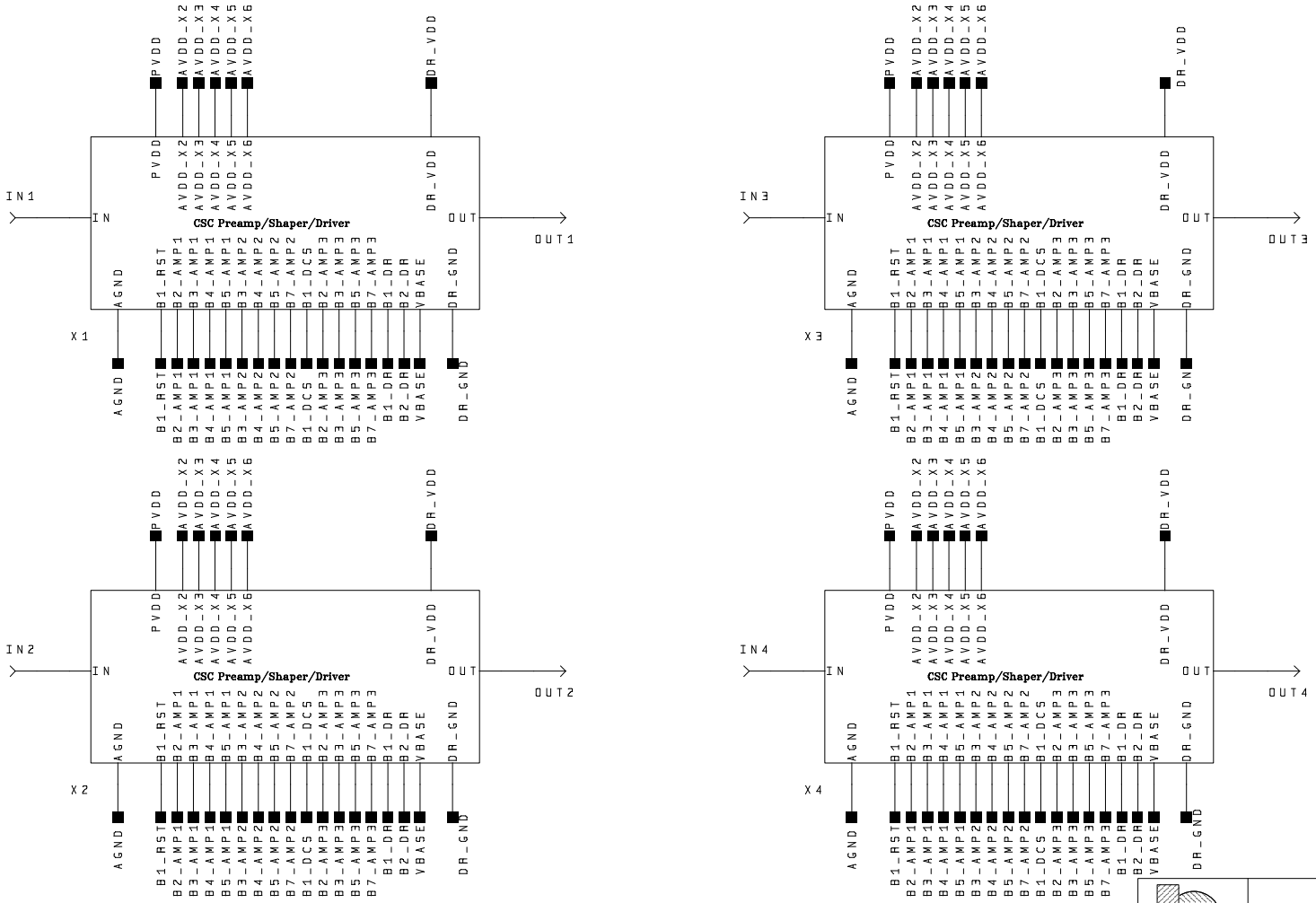
Sheet: 1 of 1



Notes:

PVDD: 3.3V
AVDD: 3.3V
DR_VDD: 3.3V
AGND: 0V
DR_GND: 0V

@DATETIME=6-7-2001_11:55
@SHEET=1

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Approvals	Date
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Checked	
Issued	
SIZE	B
DWG NO:	
REV NO:	1
SCALE	

Drawing:

ATLAS CSC / HP CMOS14TB 0.5U

CSC Preamp/Shaper 12 Channel bank

IC71

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