

Please complete and submit this ATLAS Standard Form to ATLAS RHA Coordinator ([ARC](#)), at least 2 weeks after the date of the test.

1. General information:

1.1	Date of the test:	May 17, 2003
1.2	Pre-selection, or Qualification ? (specify)	Qualification
1.3	Name of the ATLAS (or other) System:	CSC
1.4	Name of the board in the System:	ASMII
1.5	Person responsible for the test:	Sachin S Junnarkar
1.6	Institute:	BNL
1.7	Email:	sachin@bnl.gov
1.8	Person responsible for RHA of the Board:	M Dentan
1.9	Institute:	
1.10	Email:	

2. Component:

2.1	Name:	ASM2MUX
2.2	Part Number:	
2.3	Type (see section 13.1):	Digital Multiplexor
2.4	Function (see section 13.1):	Digital Multiplexing
2.5	Main specification of the component:	
2.6	Design (specify: COTS/ASIC):	ASIC
2.7	Design center (if known):	BNL
Manufacturer:		
2.8	Name of the manufacturer:	Agilent
2.9	Address of the manufacturer (if known):	
2.10	Phone of the manufacturer (if known):	
2.11	Email of the manufacturer (if known):	
2.12	Web URL of the manufacturer (if known):	
Sampling:		
2.13	Number of tested components (irradiated):	4
2.14	Number of reference components (un-irradiated):	1
Batch origin:		
2.15	Batch origin (Homogeneous/Unknown):	Homogeneous
2.16	Manufacturing date code (for homogeneous batch):	
2.17	Manufacturing line code (for homogeneous batch):	
Technology:		
2.18	Name of the technology (if known):	HP AMOS14TB
2.19	Technology (CMOS/BiCMOS/Bipolar/AsGa/Other):	CMOS
2.20	Minimum geometry (μm):	0.5
Package:		
2.21	Type:	QFP
2.22	Part number:	
2.23	Number of pin:	44
2.24	Ceramic ? Plastic ? hybrid ? (specify)	Plastic

3. Radiation:

3.1	Name of the radiation facility:	Massachusetts General Hospital
3.2	Address of the radiation facility:	Boston MA
3.3	Radiation source (see 13.2) :	Cyclotron
3.4	Radiation type (see 13.2) :	Proton (pt)
3.5	Radiation energy (MeV) :	226MeV
3.6	Minimum & maximum flux (particle per second) :	Min= 1.31e10pt/cm ² /s Max=1.61e10 pt/cm ² /s
3.7	Total fluence after last step (1 MeV eq. n/cm ²) :	Device D=1.5e13 pt/cm ² Device A=1.16e13 pt/cm ² Device E=9.49e12 pt/cm ² Device B=2.53e12 pt/cm ² at 226MeV
3.8	TID after last step (Gy) :	Device D=8.08e3 Gy Device A=6.25e3 Gy Device E=5.12e3 Gy Device B=1.36e3 Gy
3.9	Dosimetry / Calibration method:	Faraday Cup

4. Radiation test method (see 12.3):

4.1	ATLAS Standard NIEL Test Method?	Yes
4.2	Other TID test method (specify)?	

5. Thermal and voltage stresses:

5.1	Temperature (°C) :	25
5.2	Supply voltage (specify) :	3.3V
5.3	AC operation (Y/N) ?	No
5.4	If "yes" to 5.3, which AC operation?	
5.5	If "yes" to 5.3, which frequency?	

Please select and complete one or several sections among sections 6 to 9, according to the device and function(s) you are testing:

6. If your circuit is an analog circuit or contains analog functions:

6.1	Did you search for parasitic transient if any?	No
6.2	Did you record parasitic transient if any?	No
6.3	Did you search for permanent dysfunction if any?	Yes
6.4	Did you record permanent dysfunction if any?	No
6.5	Did you measure current consumption?	No
6.6	Did you record current consumption?	No
6.7	Did you perform an automatic power cycle if a permanent dysfunction or current increase occurs?	No

6.8 Description of operation and measurements of the analog (part of) circuit:
No analog part. Digital circuit only.

7. If your circuit is a digital circuit or contains digital functions:

7.1	Did you check all functions in the circuit (Y/N) ?	Yes
7.2	If “no” to 6.13, which function did you not exercise (specify) ?	
7.3	At what frequency did you exercise the circuit?	40MHz
7.4	Did you search for transient errors (Y/N) ?	Yes
7.5	Did you automatically record transient errors if any (Y/N) ?	Yes
7.6	Did you search for permanent errors (Y/N) ?	Yes
7.7	Did you automatically record permanent errors if any (Y/N) ?	Yes
7.8	Did you perform an automatic reset after a permanent error if any (Y/N) ?	No
7.9	Did you perform an automatic power cycle after a permanent error if any (Y/N) ?	No
7.10	<p>Description of operation and measurements of the digital (part of) circuit: The chip multiplexes 24 bits from 2 12 bit ADC running at 6.66MHz into 4 bits at 40MHz frequency. The chip was given a counter as an input. Its 4 bit output was compared against the expected value, using a FPGA, for errors. Errors were recorded on a 16 bit LED display, which counted the number of errors as a binary number.</p>	

8. If your circuit is a memory or a register, or contains memory(ies) or registers:

8.1	Did you check all the memories and registers of the device under test (Y/N) ?	Yes
8.2	If “no” to 8.1, which memories or registers will you not check (specify)?	
8.3	Did you search for 0 => 1 upsets (Y/N) ?	Yes
8.4	Did you search for 1 => 0 upsets (Y/N) ?	Yes
8.5	Time required to write in the memory or in the register under test?	No
8.6	After a “write” sequence, do you read the memory or register once, or periodically (answer by “once” or “each [time between 2 consecutive read]” ?	Once
8.7	After a “write” sequence, what is the time during which the memory or the register is (once or periodically) read ?	25nS
8.8	Did you automatically record bit errors if any (Y/N) ?	Yes
8.9	Did you check the “write” function of the memory or register after permanent upset if any (Y/N) ?	No
8.10	Did you perform an automatic reset after permanent upset if any (Y/N) ?	No
8.11	Did you perform an automatic power cycle after permanent upset if any (Y/N) ?	No
8.12	<p>Description of operation and measurements of the memories and/or of the registers: 24 registers latch the 24 bit data, on a rising edge of a 6.66MHz clock. These bits are then serially read out as 6 nibbles at 40MHz.</p>	

9. If your circuit is an elementary device:

Power transistors		
9.1	Did you search for burnout ignition?	NA
9.2	Did you record the rate of burnout ignition if any?	NA
Optocouplers		
9.3	Did you search for permanent dysfunction if any?	NA
9.4	Did you record permanent dysfunction if any?	NA
PIN diodes		
9.5	Did you measure the rate of parasitic transient pulses (Y/N) ?	NA
9.6	Did you record the rate of parasitic transient pulses?	NA
9.7	Description of operation and measurements of the device under test:	

10. Rejection criteria:

	Measured parameter	Rejection Criteria
10.1	Calculated Atlas Error Rate for devices RateD = 1.800×10^{-8} #errors/seconds* RateA = 1.810×10^{-8} #errors/seconds* RateE = 7.587×10^{-8} #errors/seconds* RateB = 1.423×10^{-7} #errors/seconds* *Note:refer to the supporting test report document for the calculations	>4E+4errors/sec per ASM2MUX (Acceptable error rate)
10.2	Functionality	Dysfunctional
10.3		
10.4		
10.5		

11. Results:

	11.1	11.2	11.3	11.4	11.4	11.5	11.6	11.7
	Serial number of the device Under test	number of SEU total fluence	number of bits permanently stuck total fluence	number of SEL total fluence	number of destructive SEE Total Fluence	recovery after power cycle (Y/N)?	Recovery after reset (Y/N)?	Failure mechanism (if any): for component "dead" or out of specification, give explanations and numbers
1	D	18 1.5e13	0 1.5e13	0 1.5e13	0 1.5e13	N	N	No failures
2	A	14 1.16e13	0 1.16e13	0 1.16e13	0 1.16e13	N	N	No failures
3	E	28 9.49e12	0 9.49e12	0 9.49e12	0 9.49e12	N	N	No failures
4	B	24 2.53e12	0 2.53e12	0 2.53e12	0 2.53e12	N	N	No failures

12. Comments

Use the space below to comment test results, or to report them if the above-dedicated space is inappropriate for you.

Please refer to the attached SEE test report.

13. Guidelines

13.1 Type and Function

Type	Function
Analogue device	ADC; Analogue memory; Analogue multiplexor; DAC; LVDS driver; LVDS receiver; Modulator/Demodulator; Voltage/Frequency converter
Data transmission Component	Receiver; Transceiver; Transmitter
Front-end electronic device	Drift Time Measurement; Multiple functions; Readout memory
Linear device	Amplifier; Comparator; Operational amplifier; Voltage reference;
Memory	SRAM
Microprocessor or peripheral	Microcontroller; Microprocessor
Optoelectronic component	Laser; Light emitting diode – LED; PIN diode; VCSEL
Power device	DC-DC converter; Power transistor; Voltage regulator
Programmable device	EEPROM; FPGA; Lookup table; Programmable delay
Passive component	Capacitor
Interfaces/Communication	LVDS; Switch
Mixed A/D device	Multiple functions
Logic gates	NOR, NAND, etc.

13.2 Radiation source and type

Source of radiation	Type of radiation
Accelerator	Electron, proton, spallation neutron
Am-241	Ions (fission products)
Cf-252	Ions (fission products)
Co-60	Photon gamma 1.173 MeV and 1.332 MeV
Cs-137	Photon gamma 0.662 MeV
Cyclotron	Proton, ion (specify), spallation neutron
Reactor	Neutron
Tandem accelerator	Protons, ions
Van-de-Graaf	Electron
X-Ray generator	Photon X

13.3 Radiation test methods:

see ATLAS Policy on Radiation Tolerant Electronics rev. 2, pp. 20-26

http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/ATLASPolicy/APRTE_rev2_250800.pdf

Single Event Effects Test report for ASM2MUX

This document describes the test setup used and the procedure for SEE testing at Massachusetts General Hospital, cyclotron facility of the ASM2MUX chips, for ASMII boards which are a part CSC on chamber electronics,

Introduction:

ASMII Boards have 16, 12 bit ADCs, running at 6.66MHz. Data from these ADCs is transmitted on 2 optical fibers to the ROD via 2, 16 bit G-Link transmitters, which run at 40MHz. In order to multiplex data from these 16 ADCs, 8 ASM2MUX chips are used. Each ASM2MUX multiplexes 24 bits from 2, 12 bit ADC running at 6.66MHz into 4 bits at 40MHz frequency, thereby generating two 16bit words, for the G-Link. For a detail study please refer to the ASM2MUX schematic. This is an ASIC designed at BNL and fabricated in HP 0.5 μ process titled HP AMOS14TB, in CMOS technology. There will be 320 ASMII and 2560 ASM2MUX for the complete CSC system.

Test Setup:

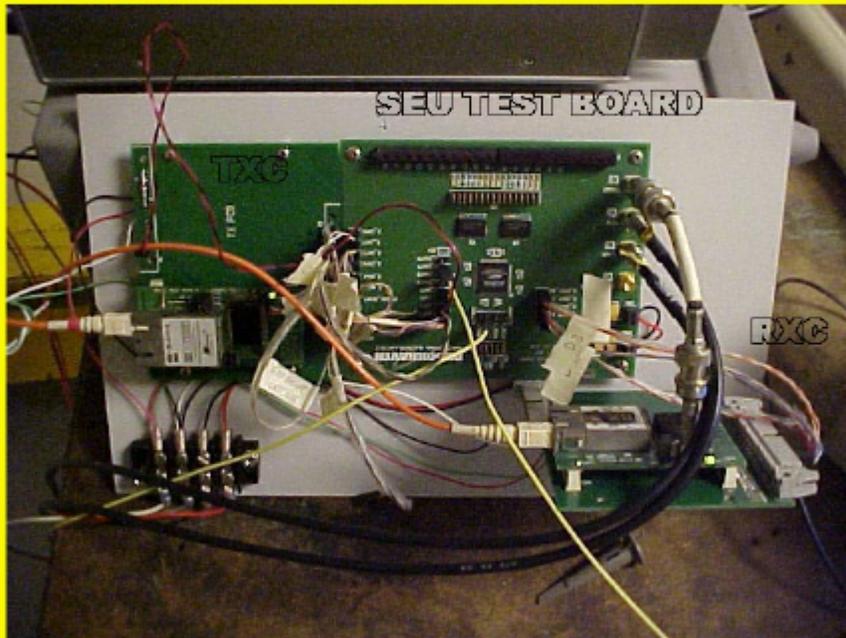
The test setup consisted of two modules, counting room module and the beam area module, interconnected via two 50 ft optical fibers. The counting room module included SEU test board, 1 G-Link transmitter board (TXC) (HDMP-1022, and Stratos Lightwave optics), and 1 G-Link receiver (RXC) (HDMP-1024 and Stratos Lightwave optics) board. The beam area module had DUT board, and similar, 1G-Link transmitter (TXB) board and 1 G-Link receiver (RXB) board. 4 bit test pattern for the Device Under Test (DUT) was generated inside an FPGA on the SEU Test Board, at 40MHz. This 4 bit test pattern and 6.66MHz clock needed for the DUT were transmitted to the beam area on a fiber as 5 G-Link data bits. 40MHz clock was extracted from the STRBOUT pin of the RXB was fed to the DUT and was also used as STRBIN for the TXB. These 4 bits were fed to DUT as 6 nibble input to make all the 24 input bits toggle at the same time, giving the maximum variation at the inputs. 4bit DUT output was transmitted back to the counting room using 4 data bits of the TXB. This 4 bit data was compared with the output of a dummy ASM2MUX inside an FPGA, which had the same inputs as DUT. The error counter was incremented by 1 every time the 4bit comparator yielded a mismatch. These errors were displayed as a 16bit binary number, using 16LEDs. All the DUTs were tested using the same setup before being irradiated for prolonged intervals. No errors were recorded.

Procedure:

The beam area module was placed in the beam path so that the DUT will be perpendicular to the beam, and at a calibrated distance. Faraday cup was used for calibration. G-Links were getting a considerable dose, and were found to lose lock frequently (consistent with the G-Link radiation tests done before*). Two lead bricks each were placed to shield RXB and TXB. This was an effective solution and the G-

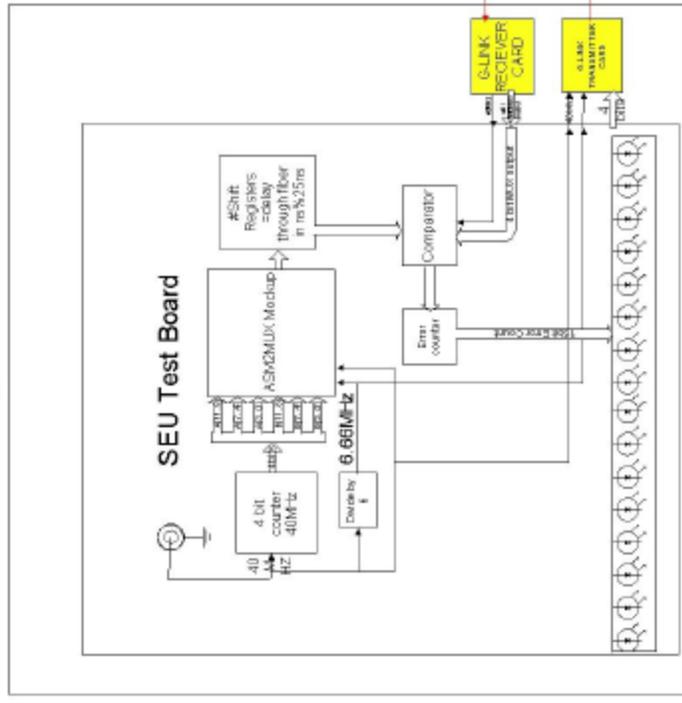
Links lost lock less frequently with this setup. Every lost lock event needed power cycling of the test setup to get the G-links to lock again. Error LEDs were monitored using a CCD camera on a monitor in the control room. 4 devices were tested. The results from the tests are attached with this document. Similar setup was reconstructed back at BNL for testing the cooled off devices to test for any permanent stuck bits and destructive SEEs. No errors were reported in these post radiation tests.

ERROR MONITOR LEDs

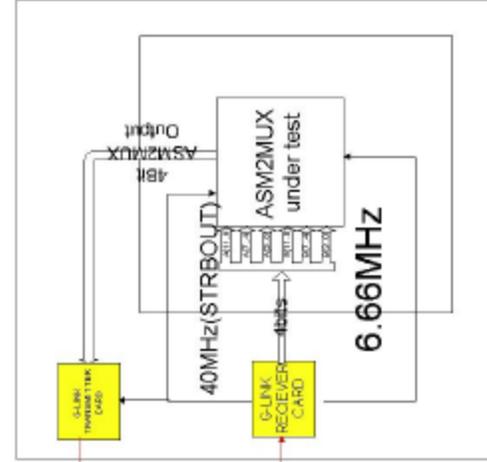


COUNTING ROOM MODULE

Counting Room

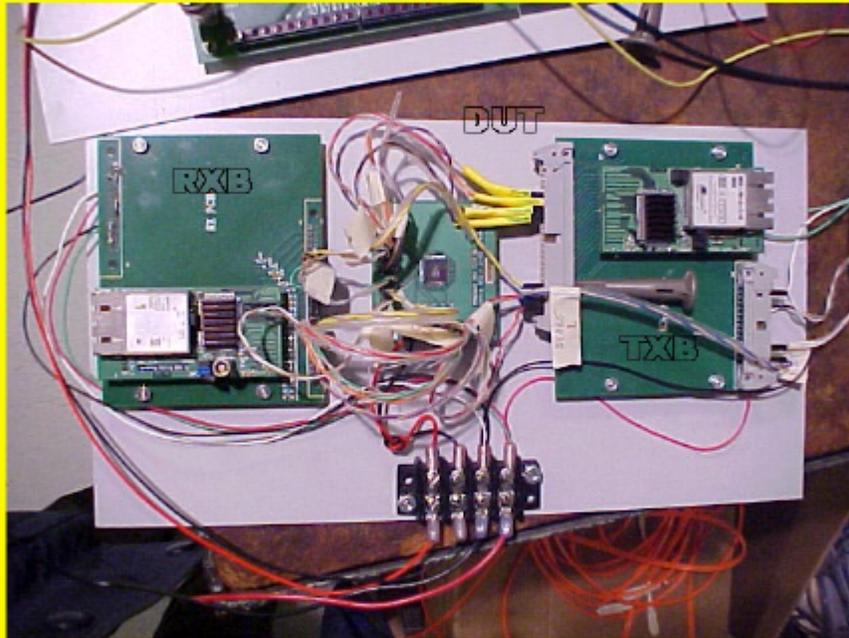


Beam Area



SEE Test Setup for ASM2MUX

Sachin Shrirang Junnarkar .
July 9, 2003



BEAM AREA MODULE

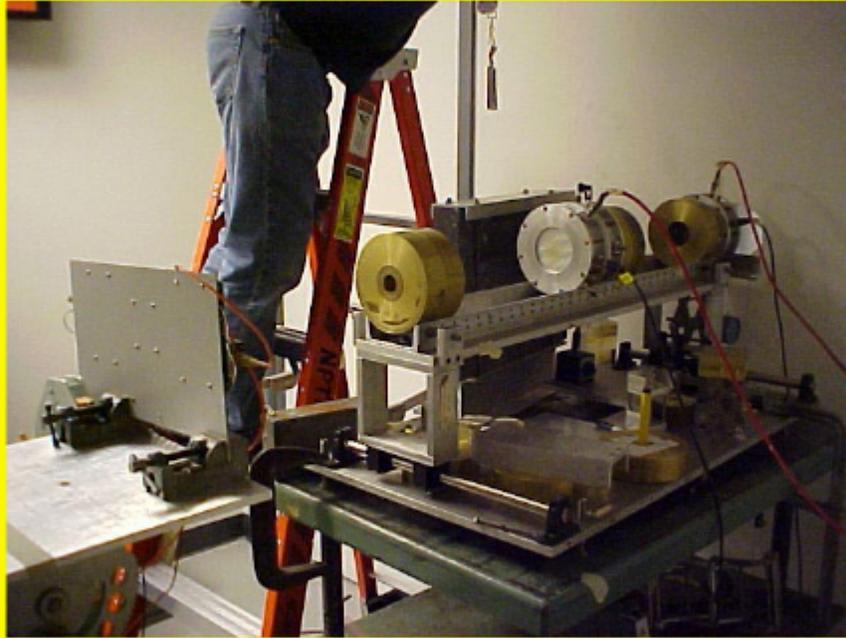
ERROR MONITOR



BEAM AREA MONITOR

LEWAD Bechtel Corporation July 1998 and 1999 beam line system

BEAM SETUP



BEAM AREA MODULE

Acceptable CSC error rates:

Considering CSC chamber inefficiency of 2%, and aiming for a 1% inefficiency in the electronics following statistics holds true:

For the full CSC system suppose a track's data consists of 4 layers, (5x+1Y=6) strips/layer 4 time samples, 12 bits/sample = $4 \times 6 \times 4 \times 12 = 1152$ bits.

For each track (event) the whole CSC needs to be readout. Each CSC consists of 5 ASMIIIs, with 192 strips each.

The total data bits read per event=46080bits.

Probability of a any given bit being a track data bit $P_t = 1152/46080 = 1/40$

1 corrupted bit in 115200bits, would cause 1%data loss if every bit belonged to a track. Only $1152/46080 = 1/40$ bits belong to a track.

Therefore 1 corrupted bit in $115200/40 = 2880$ bits is acceptable.

CSC readout time is 10us per event. Giving CSC data rate = $46080/10E-6 = 4.608$ GBPS.

1 corrupted bit in 2880 => $4.608E+9$ bits/second

$$\frac{\text{-----}}{2880 \text{ bits}} = 1.6E+6 \text{ errors/second per CSC}$$

There are 40 ASM2MUXs per CSC

Allowed rate per mux

= $1.6E+6$ errors/second per CSC

$$\frac{\text{-----}}{40 \text{ muxes per CSC}} = 4E+4 \text{ errors/second per ASM2MUX}$$

Single Event Upset Rate for CSC ASM2MUX

ATLAS Simulated Radiation Level

SRL:= $1.5 \cdot 10^{12}$ protons/cm²

LHC integrated beam time in 10 years:= 10^8 seconds

Total number of ASM2MUX in CSC

NUM_{mux} := 2560

SEU Cross-Section for ASM2MUX

$X_{\text{sec}}(\text{Errors, Fluence}) := \frac{\text{Errors}}{\text{Fluence}} \quad \text{cm}^2/\text{proton}$

Applied Fluence Observed SEU errors

AF _D := $1.5 \cdot 10^{13}$	Err _D := 18
AF _A := $1.16 \cdot 10^{13}$	Err _A := 14
AF _E := $9.49 \cdot 10^{12}$	Err _E := 48
AF _B := $2.53 \cdot 10^{12}$	Err _B := 24

CrossSectionD = 1.200×10^{-12} cm²/protons

CrossSectionA = 1.207×10^{-12} cm²/protons

CrossSectionE = 5.058×10^{-12} cm²/protons

CrossSectionB = 9.486×10^{-12} cm²/protons

SEU Error Rate per ASM2MUX device

$$\text{SEU}_{\text{rate}}(X_{\text{sec}}, \text{SRL}, \text{LHC}_{\text{time}}) := \frac{X_{\text{sec}} \cdot \text{SRL}}{\text{LHC}_{\text{time}}} \text{ #errors/seconds}$$

$$\underline{\text{RateD} = 1.800 \times 10^{-8} \text{ #errors/seconds*}}$$

$$\underline{\text{RateA} = 1.810 \times 10^{-8} \text{ #errors/seconds*}}$$

$$\underline{\text{RateE} = 7.587 \times 10^{-8} \text{ #errors/seconds*}}$$

$$\underline{\text{RateB} = 1.423 \times 10^{-7} \text{ #errors/seconds*}}$$

*Refer to acceptable error rate per ASM2MUX=4E+4errors/seconds

SEU Error Rate for the Entire CSC system

$$\text{SEU}_{\text{system}}(\text{Rate}, \text{Devices}) := \text{Rate} \cdot \text{Devices} \text{ #errors/seconds}$$

$$\text{SEU}_{\text{SYSTEMD}} = 4.608 \times 10^{-5} \text{ #errors/seconds}$$

$$\text{SEU}_{\text{SYSTEMA}} = 4.634 \times 10^{-5} \text{ #errors/seconds}$$

$$\text{SEU}_{\text{SYSTEME}} = 1.942 \times 10^{-4} \text{ #errors/seconds}$$

$$\text{SEU}_{\text{SYSTEMB}} = 3.643 \times 10^{-4} \text{ #errors/seconds}$$

Time Interval between 1 SEU events in the CSC system due to ASM2MUX

$$\text{Interval}_{\text{SEU}}(\text{SEU}_{\text{RATE}}) := 1/\text{SEU}_{\text{RATE}} \text{ SECONDS}$$

$$\text{IntervalD} = 21701 \text{ seconds}$$

$$\text{IntervalA} = 21577 \text{ seconds}$$

$$\text{IntervalE} = 5149 \text{ seconds}$$

$$\text{IntervalB} = 2745 \text{ seconds}$$

SUMMARY

Single Even Upset Rate for CSC ASM2MUX					
SRL	1.50E+12	>20 MeV Hadrons/cm² for 10 years			
LHCtime	1.00E+08	seconds for 10 years			
Acceptable error rate	4E+4errors/sec				
ASM2MUX count	2560				
MUXID	D	A	E	B	
Applied Fluence (Protons/cm ²)	1.50E+13	1.16E+13	9.49E+12	2.53E+12	
Total Errors	18	14	28	24	
SEU X-Section/MUX	1.20E-12	1.21E-12	2.95E-12	9.49E-12	
SEU Error Rate/MUX	1.80E-08	1.81E-08	4.43E-08	1.42E-07	
SEU X-Section for CSC due to MUX	4.61 E-05	4.63E-05	1.13E-04	3.64E-04	
1 SEU occurs in the system from the MUX every minutes	361.7	359.6	147.1	45.8	

Conclusion:

From the table above it can be seen that all the tested ASM2MUXs show error rates, which are far better than the acceptable CSC error rates. For comparison the worst case observed rate for the four devices, is $1.423\text{E-}6$ errors/second for device "B" as compared to the acceptable rate for the ATLAS experiment, which is $4\text{E+}4$ errors/second per ASM2MUX. Also the post radiation tests after SEE show that the devices are fully functional and show no permanently stuck bits as well as no destructive SEUs. Post radiation results for TID and NEIL also show that ASM2MUX performs well under those conditions*.

**Refer to the NEIL and TID standard test reports submitted along with this document for details.*