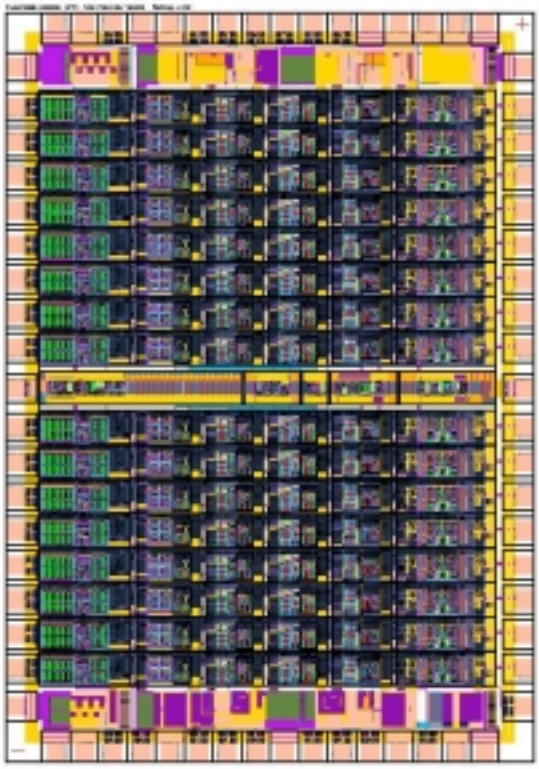
ATLAS Cathode Strip Chamber
Preamplifier Shaper Integrated Circuit (IC50)
Prototype Test Results (April 2001)

Specifications:

Channel count : 16
Process: Agilent Technologies 0.5µm AMOS14TB Process
Gain: 4 mV/fC
Shaping: 70ns/Bipolar
Die size: 2.78mm x 3.95mm



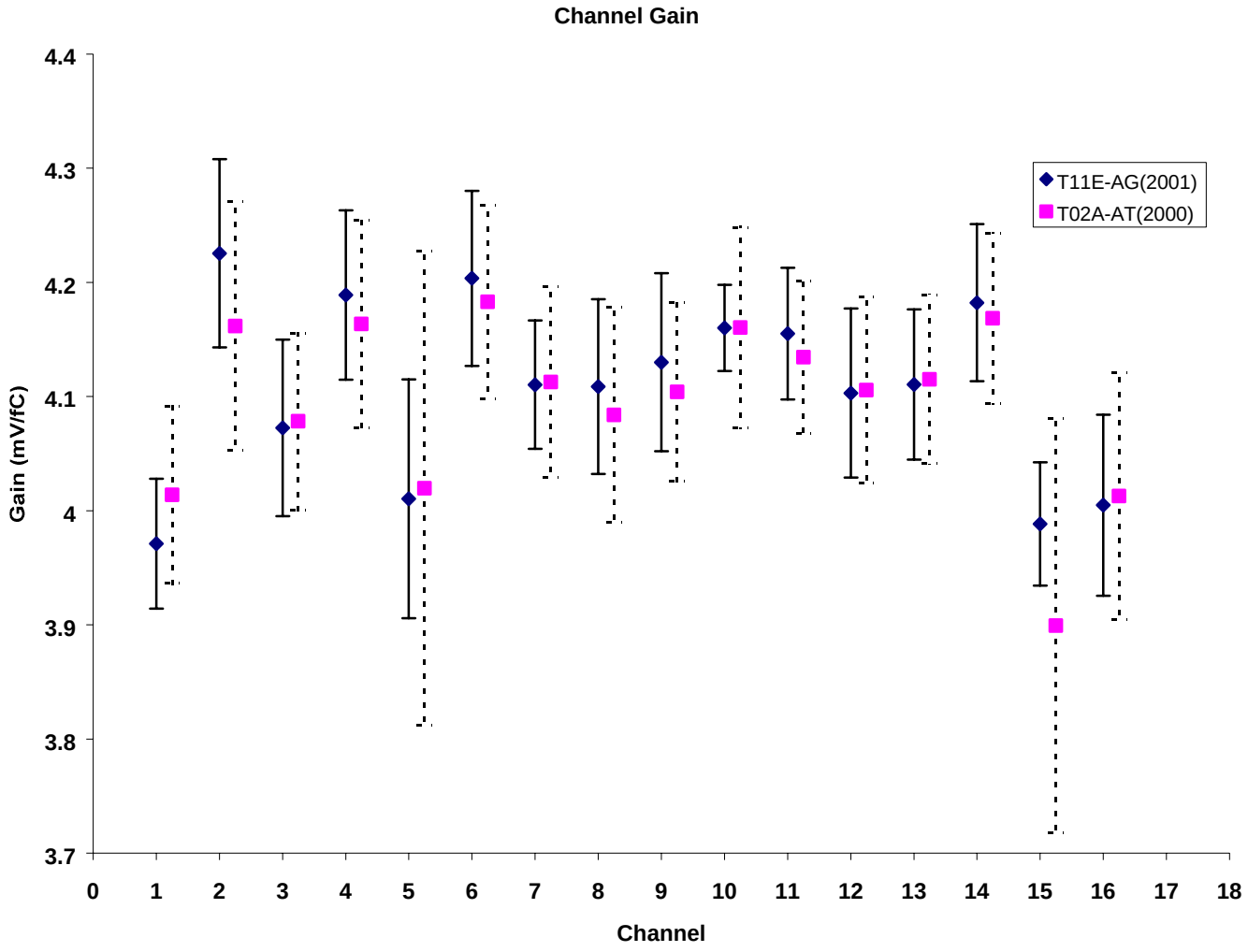
Prototyping Runs:

RUN ID	YEAR	QTY
N95C-AR	2Q – 1999	25
T02A-AT	1Q – 2000	32
T11E-AG	1Q – 2001	25

Anand Kandasamy
anand@bnl.gov

Gain:

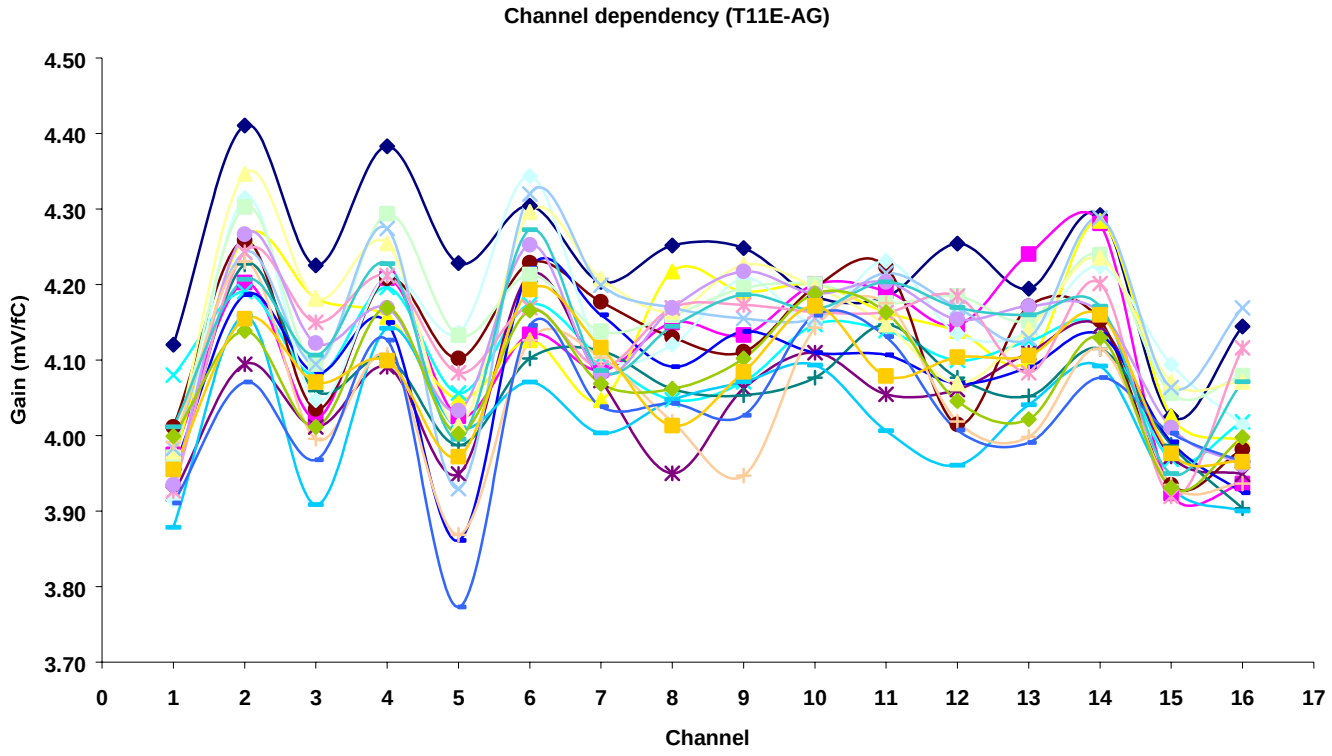
	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15	Ch16
T11E	3.97	4.23	4.07	4.19	4.01	4.20	4.11	4.11	4.13	4.16	4.16	4.10	4.11	4.18	3.99	4.00
	1.43%	1.95%	1.90%	1.77%	2.61%	1.82%	1.37%	1.86%	1.89%	0.91%	1.39%	1.81%	1.60%	1.64%	1.35%	1.98%
T02A	4.01	4.16	4.08	4.16	4.02	4.18	4.11	4.08	4.10	4.16	4.13	4.11	4.12	4.17	3.90	4.01
	1.93%	2.62%	1.90%	2.18%	5.16%	2.03%	2.03%	2.31%	1.91%	2.11%	1.61%	1.99%	1.80%	1.79%	4.66%	2.70%

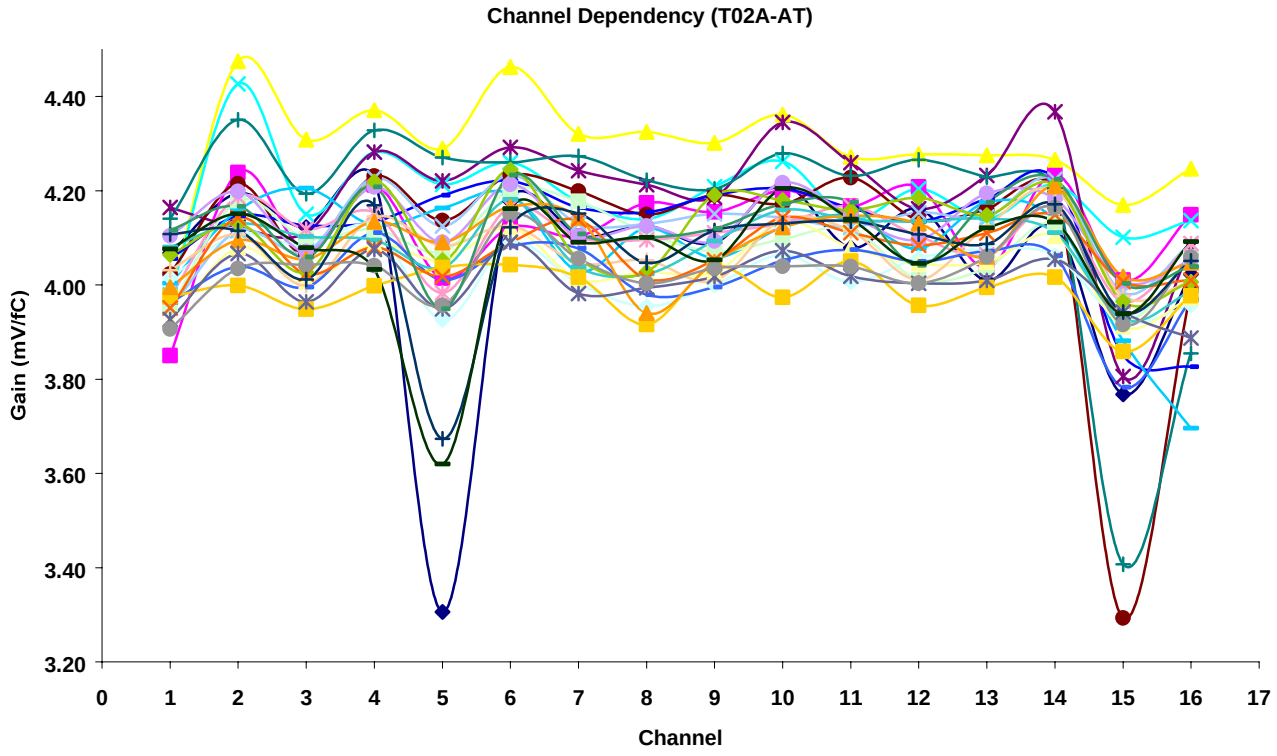


Worst case measured Standard Deviation channel to channel:

T11E-AG : 2.67%
T02A-AT : 5.57%

Anand Kandasamy
anand@bnl.gov

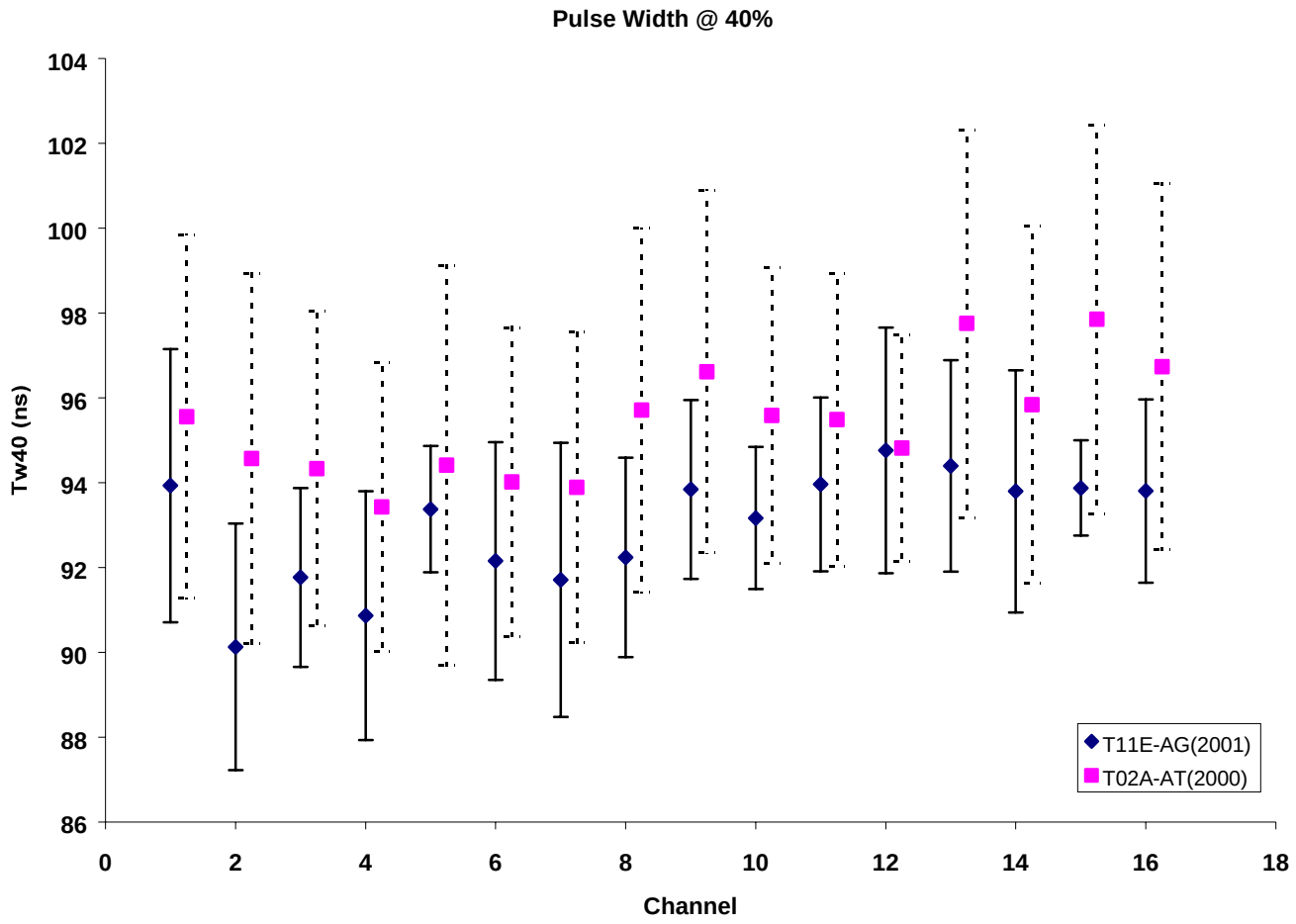




Anand Kandasamy
anand@bnl.gov

Pulse width at 40% of pulse height:

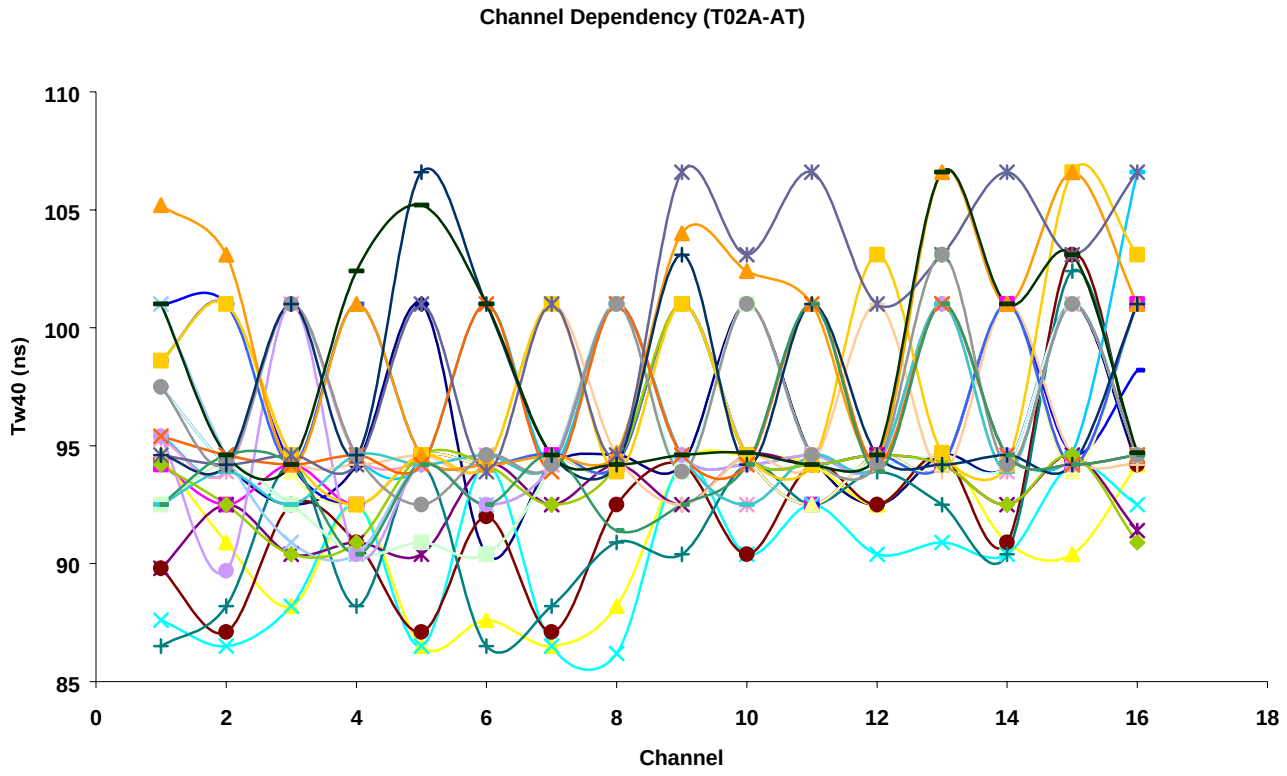
	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15	Ch16
T11E	93.93	90.13	91.77	90.87	93.38	92.16	91.71	92.24	93.84	93.17	93.96	94.76	94.40	93.80	93.88	93.81
	3.43%	3.22%	2.30%	3.23%	1.60%	3.04%	3.52%	2.55%	2.25%	1.80%	2.18%	3.06%	2.64%	3.05%	1.20%	2.30%
T02A	4.01	4.16	4.08	4.16	4.02	4.18	4.11	4.08	4.10	4.16	4.13	4.11	4.12	4.17	3.90	4.01
	4.48%	4.61%	3.93%	3.65%	4.98%	3.87%	3.90%	4.47%	4.42%	3.65%	3.62%	2.82%	4.67%	4.40%	4.68%	4.46%

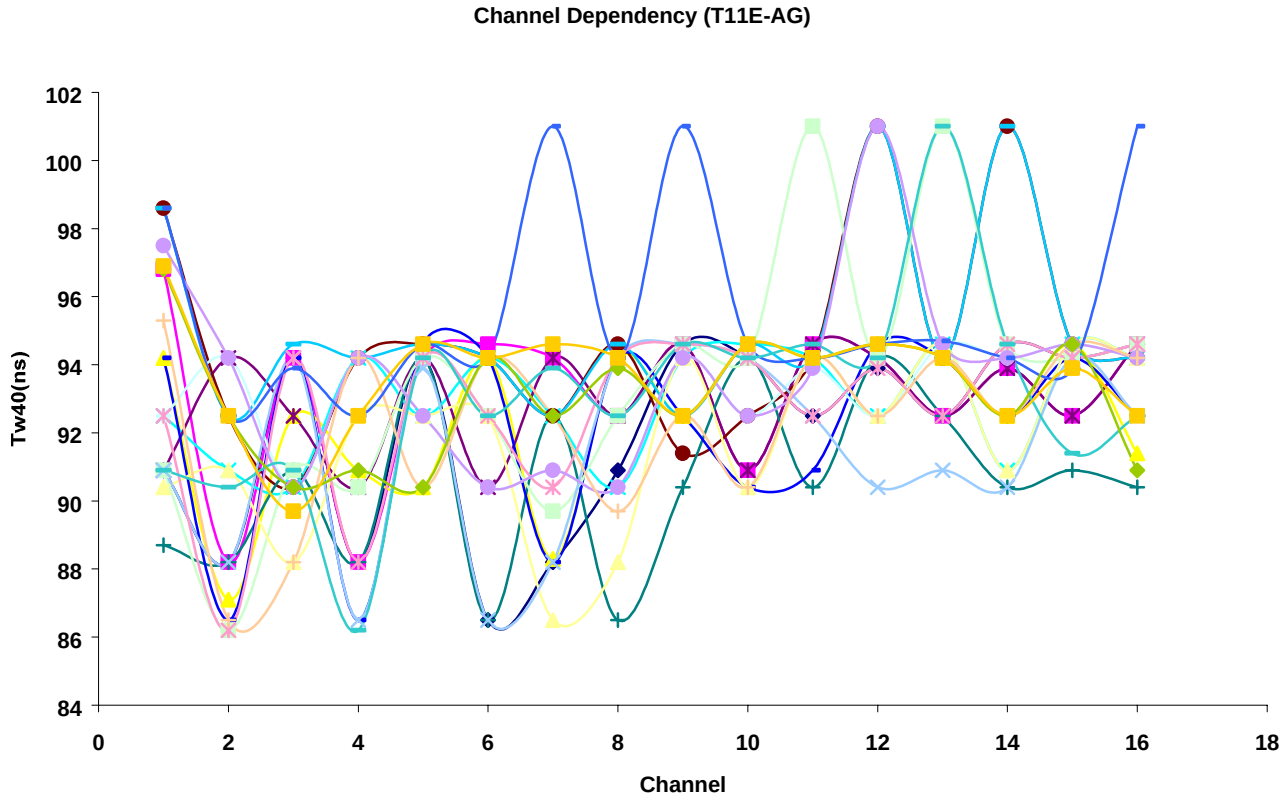


Worst case measured Standard Deviation channel to channel:

T11E-AG : 4.01%
T02A-AT : 5.13%

Anand Kandasamy
anand@bnl.gov

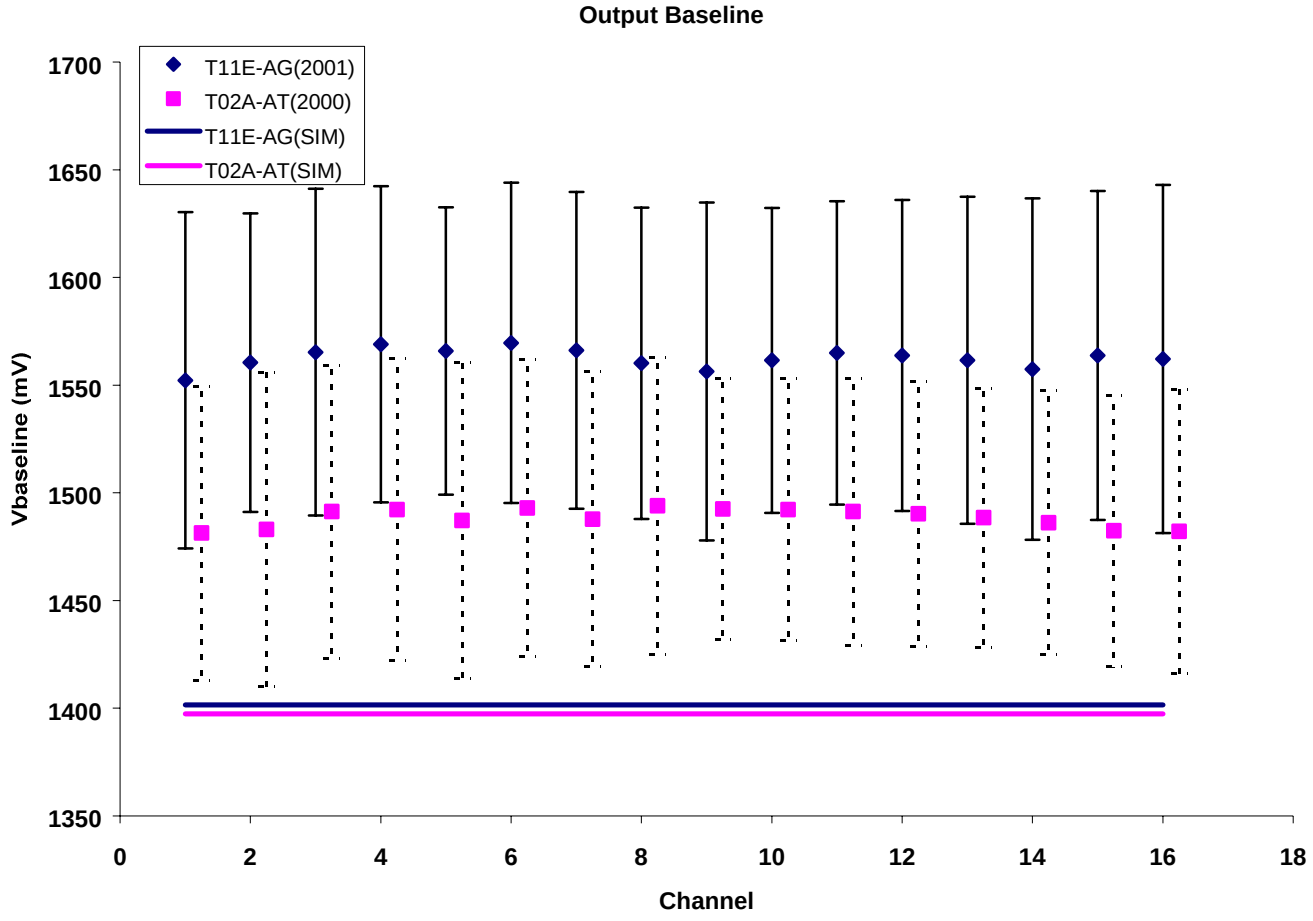




Anand Kandasamy
anand@bnl.gov

Output Baseline:

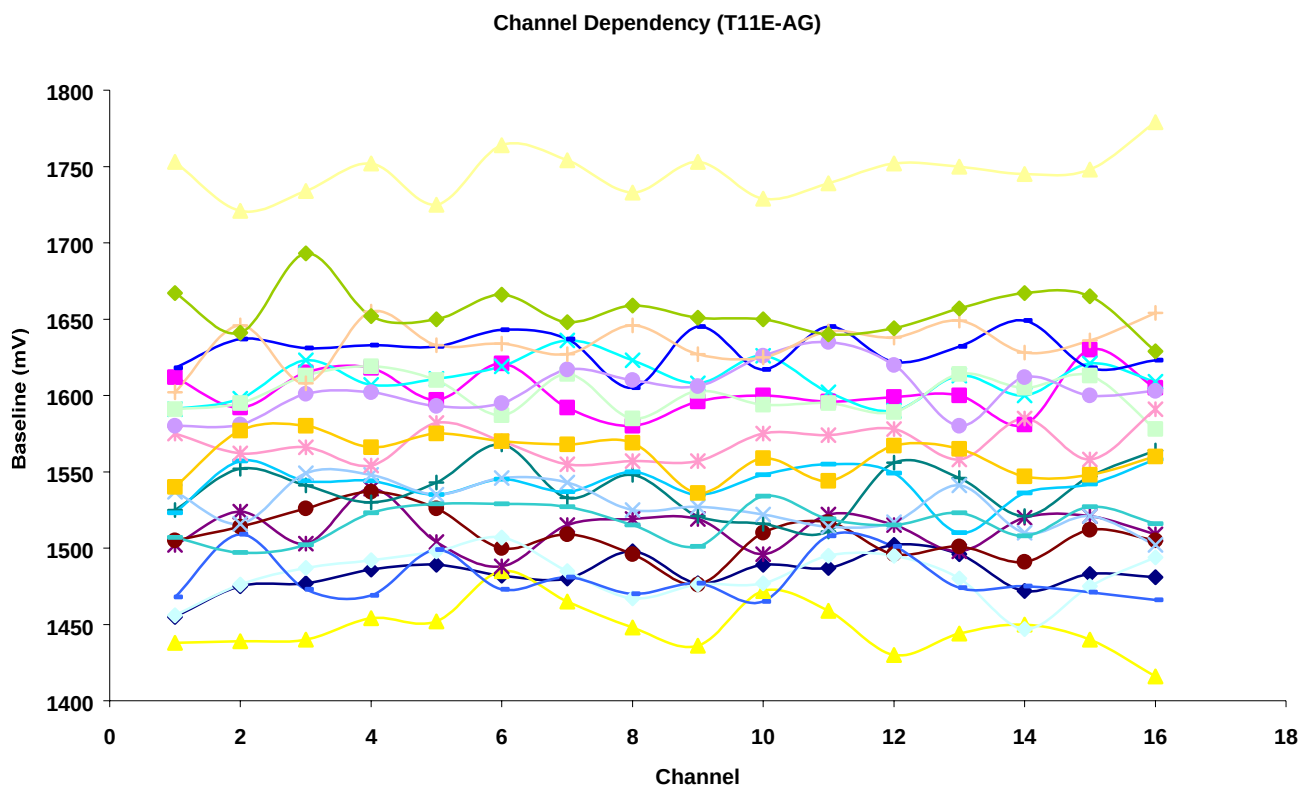
	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15	Ch16
T11E	1552.3	1560.5	1565.3	1569.0	1565.9	1569.6	1566.2	1560.2	1556.4	1561.5	1565.0	1563.8	1561.6	1557.5	1563.8	1562.1
	5.03%	4.44%	4.85%	4.67%	4.26%	4.74%	4.69%	4.63%	5.04%	4.54%	4.50%	4.61%	4.86%	5.08%	4.88%	5.17%
T02A	1481.3	1483.0	1491.3	1492.1	1487.1	1492.9	1487.7	1493.9	1492.4	1492.2	1491.3	1490.3	1488.5	1486.1	1482.3	1482.1
	4.61%	4.90%	4.57%	4.69%	4.93%	4.62%	4.60%	4.62%	4.07%	4.09%	4.16%	4.12%	4.04%	4.13%	4.25%	4.44%

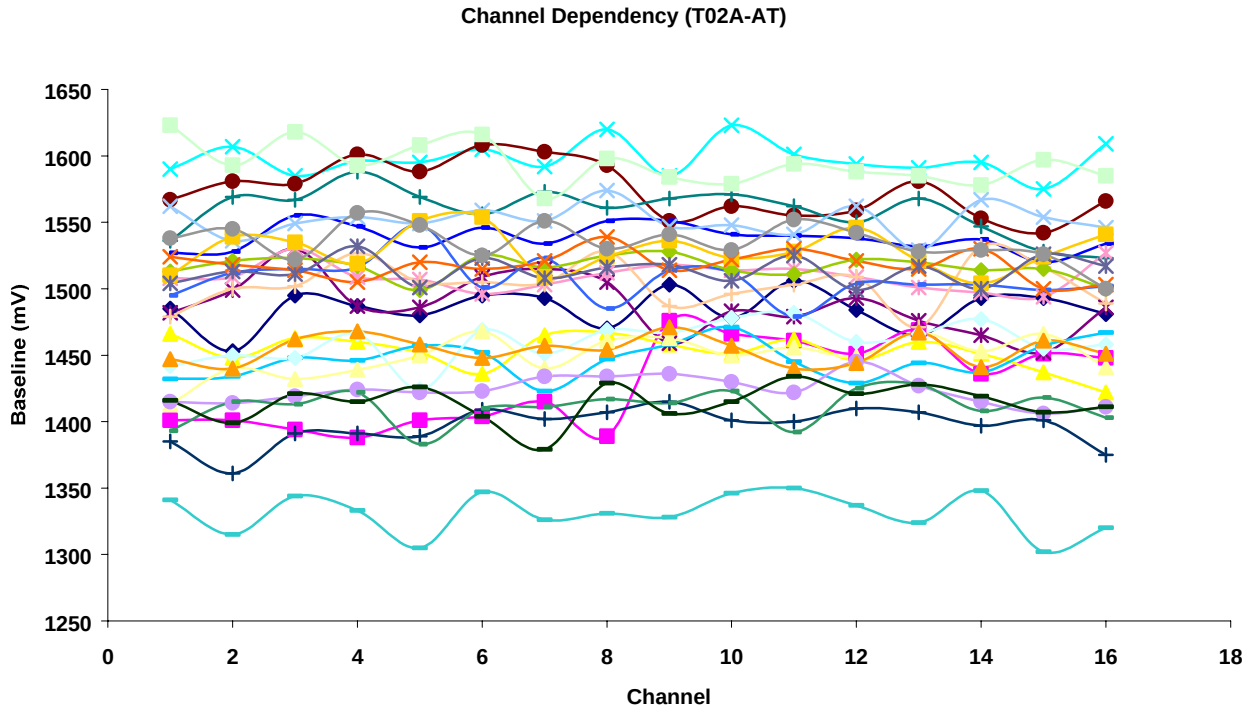


Worst case measured Standard Deviation channel to channel:

T11E-AG : 1.16%
T02A-AT : 2.23%

Anand Kandasamy
anand@bnl.gov

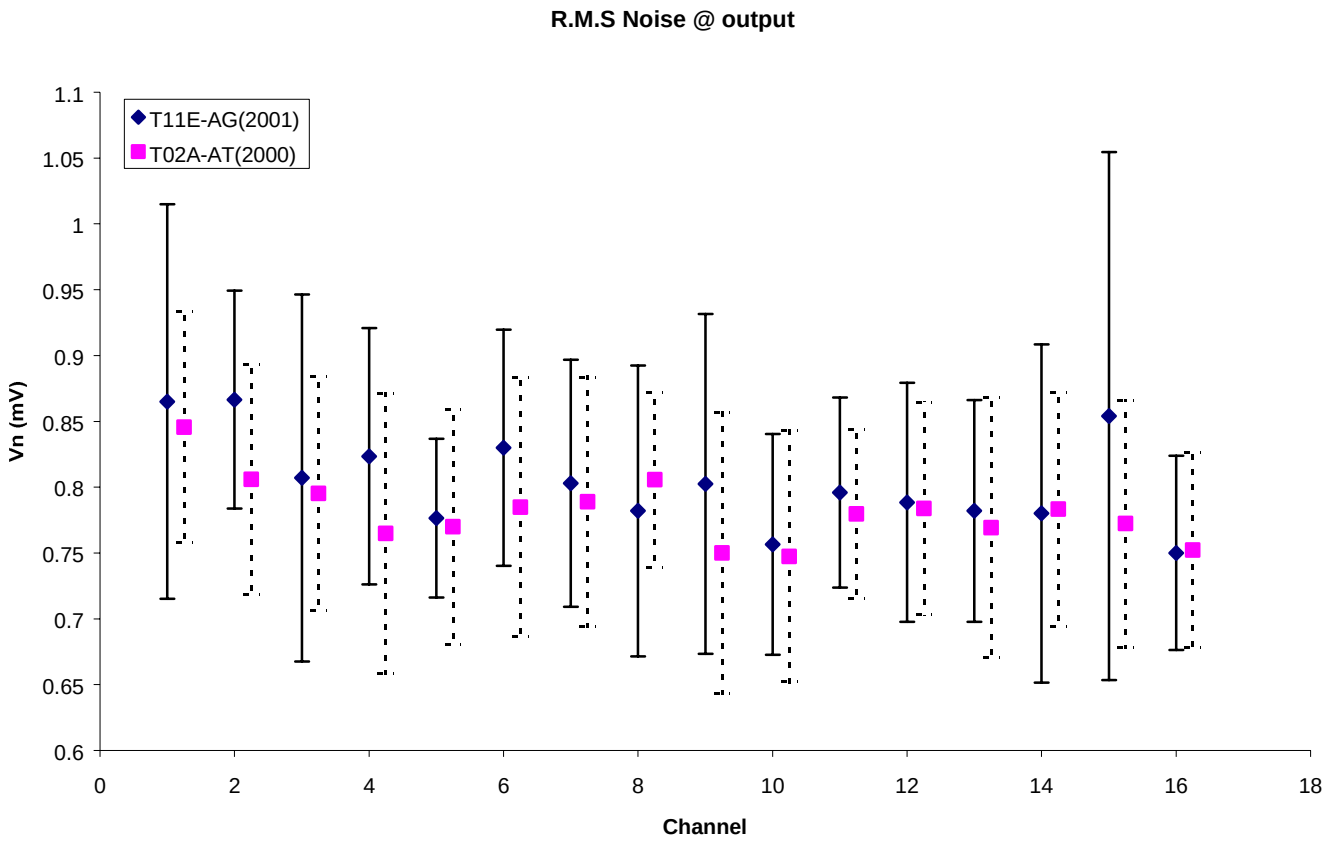




Anand Kandasamy
anand@bnl.gov

R.M.S Noise at the output (No detector capacitance):

	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15	Ch16
T11E	0.87	0.87	0.81	0.82	0.78	0.83	0.80	0.78	0.80	0.76	0.80	0.79	0.78	0.78	0.85	0.75
	17%	10%	17%	12%	8%	11%	12%	14%	16%	11%	9%	12%	11%	16%	23%	10%
T02A	0.85	0.81	0.80	0.76	0.77	0.78	0.79	0.81	0.75	0.75	0.78	0.78	0.77	0.78	0.77	0.75
	10%	11%	11%	14%	12%	13%	12%	8%	14%	13%	8%	10%	13%	11%	12%	10%

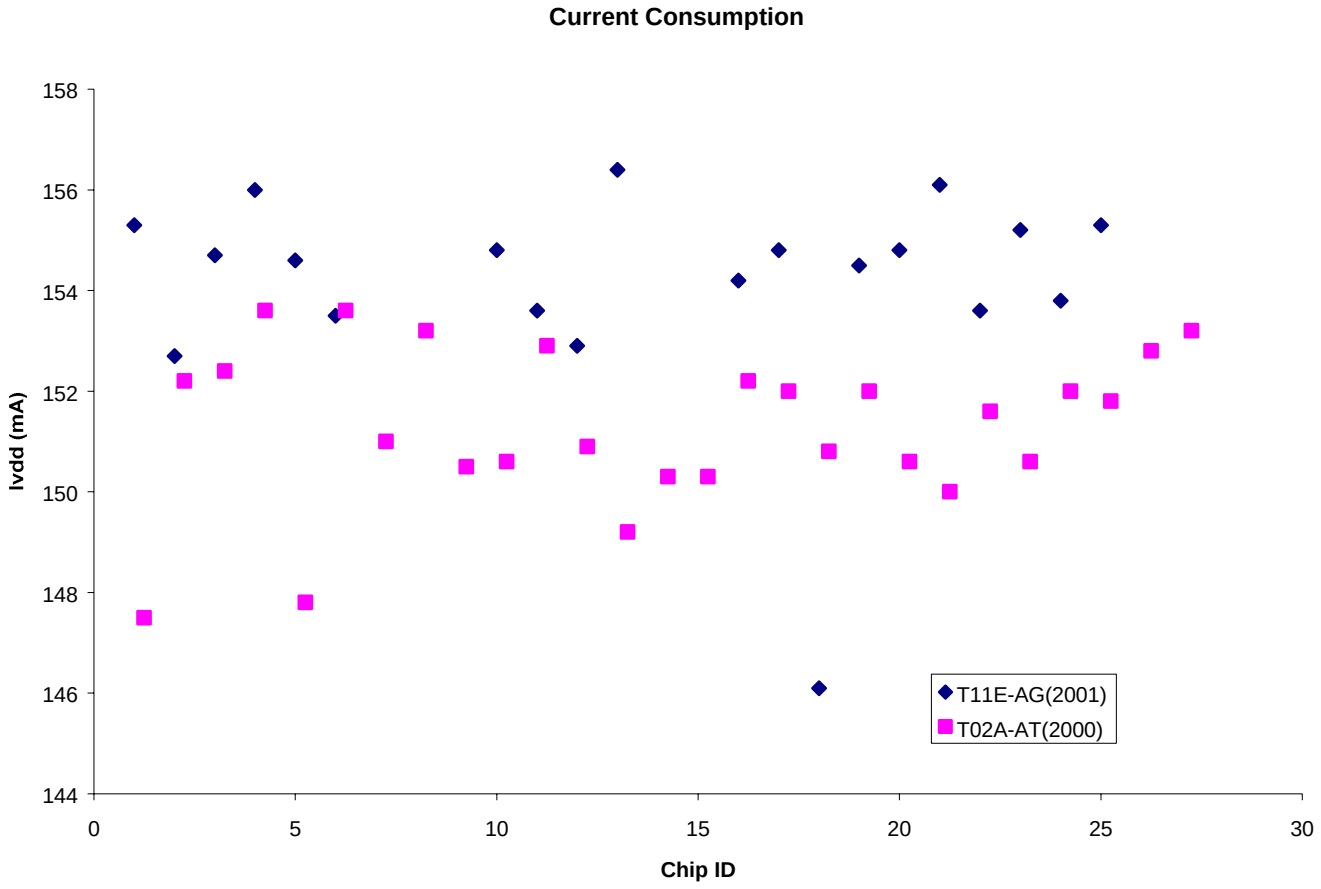


Worst case measured Standard Deviation channel to channel:

T11E-AG : 24.2%
T02A-AT : 16.1%

Anand Kandasamy
anand@bnl.gov

Power :



In lot Chip to Chip variation:

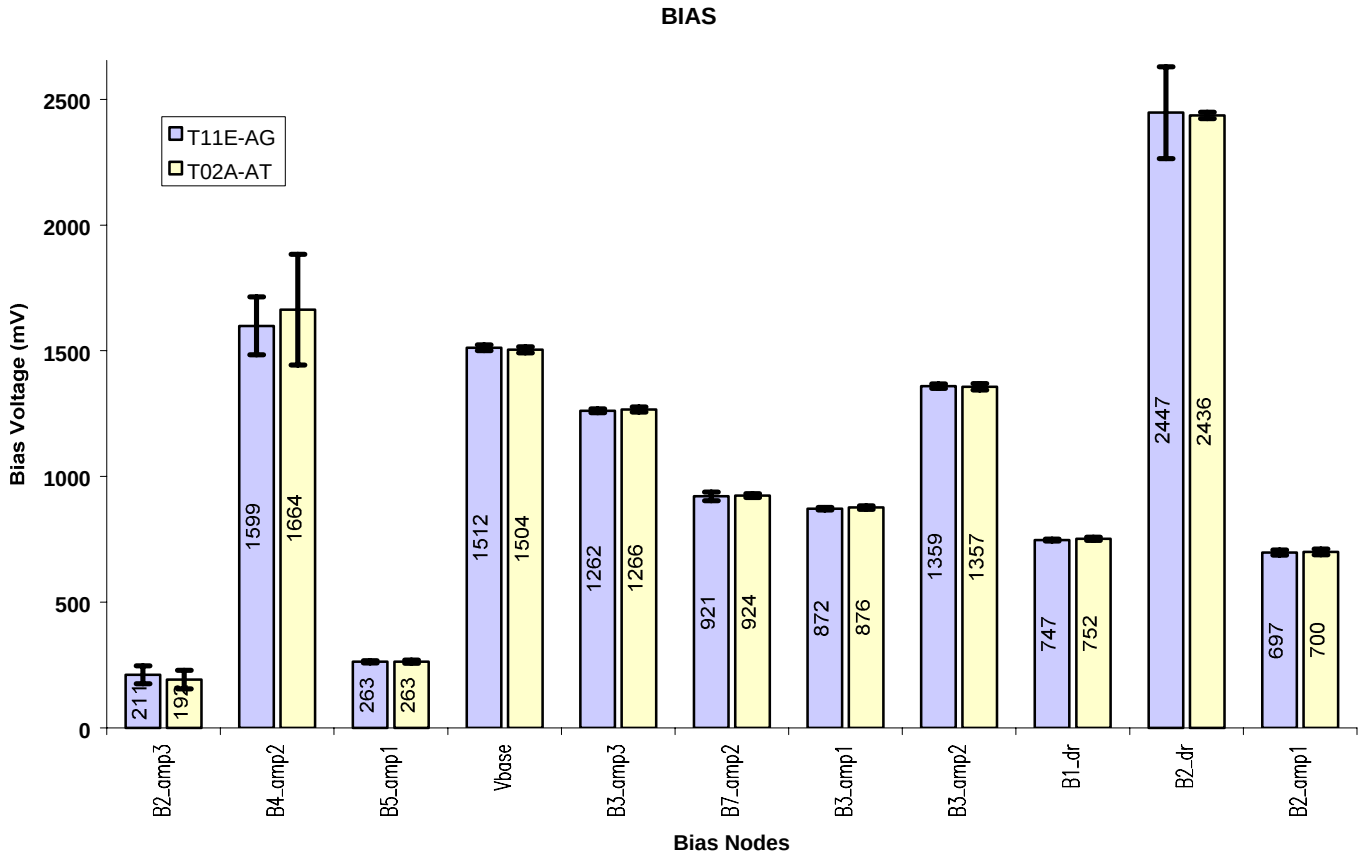
Lot T11E-AG : 1.39% (mean: 154.1mA)
Lot T02A-AT: 1.04% (mean: 151.3mA)

Lot to Lot Variation: 1.51% (mean: 152.5mA)

Anand Kandasamy
anand@bnl.gov

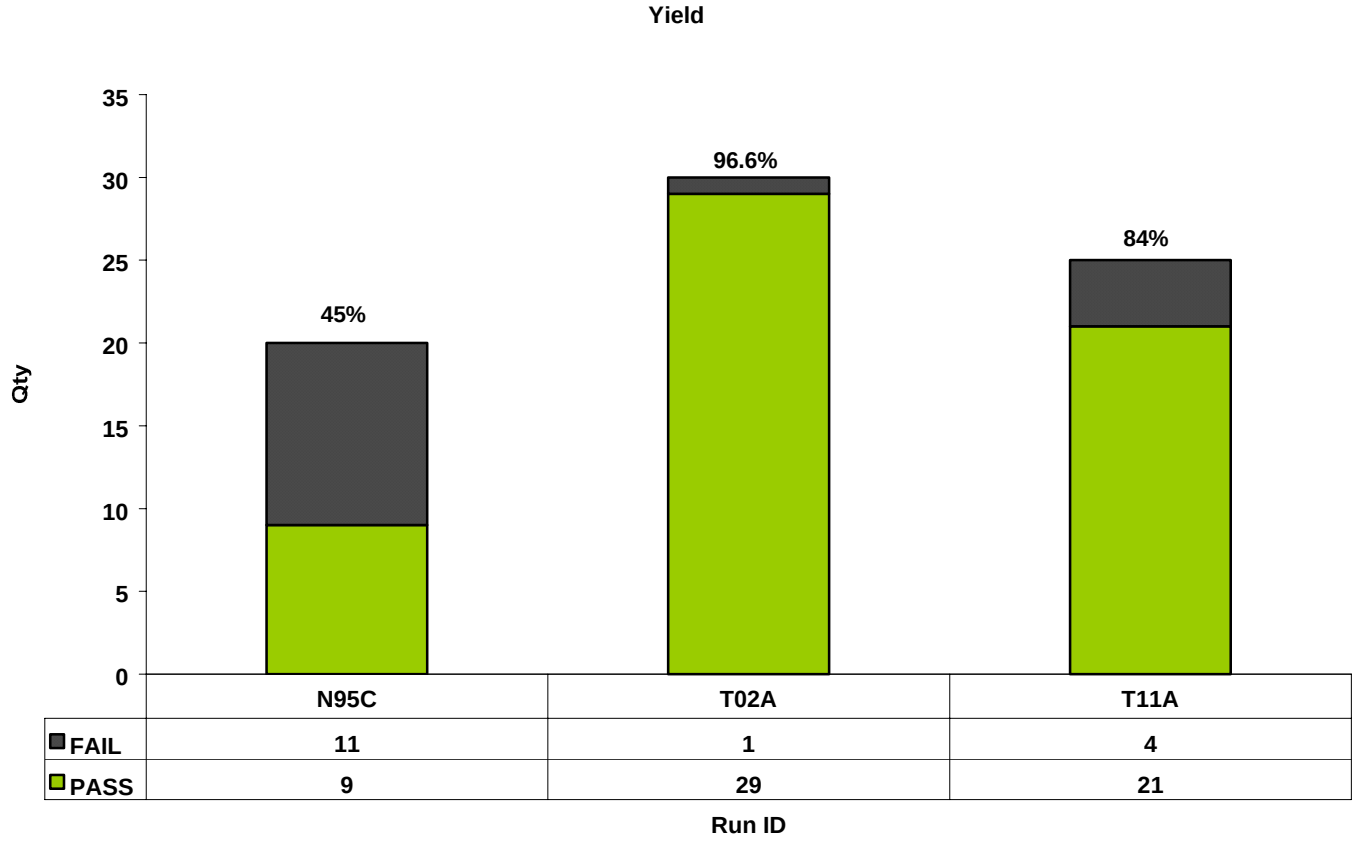
Bias Voltages:

	B2_amp3	B4_amp2	B5_amp1	Vbase	B3_amp3	B7_amp2	B3_amp1	B3_amp2	B1_dr	B2_dr	B2_amp1
T11E	211.45	1599.05	262.85	1512.45	1261.5	920.85	871.65	1359.25	747.3	2447.1	697.05
	16.92%	7.18%	1.89%	0.75%	0.63%	1.92%	0.58%	0.63%	0.56%	7.46%	1.45%
T02A	191.85	1663.52	263.30	1504.15	1266.33	924.26	876.41	1356.59	752.22	2435.89	699.96
	19.2%	13.2%	2.5%	0.8%	0.8%	0.8%	0.8%	0.9%	0.8%	0.5%	1.7%



Anand Kandasamy
anand@bnl.gov

Yield:



Cumulative yield : 78.8%

Anand Kandasamy
anand@bnl.gov

Failure modes:

BIAS	Failures		Cbias	Cbias_ext	Cbias_total	TYPE
b2_amp1	4	VDD	100	95	195	2P
b2_amp3	3	VDD	17	85	102	1N
b2_dr	3	VDD	30	85	115	1P
b7_amp3	2	GND	17	50	67	1P
b1_dcs	2	GND	22	125	147	1P
b3_amp1	2	GND	30	50	80	1P
b3_amp3	2	GND	17	125	142	1P
b5_amp1	2	VDD	100	85	185	2P
b5_amp2	1	VDD	10	85	95	1P
b5_amp3	1	VDD	10	125	135	1N
b1_dr	1	GND	29	50	79	1P
b4_amp2	1	VDD	15	50	65	1N
b3_amp2	0	GND	15	50	65	1P
b1_rst	0	GND	10	16	26	-
b4_amp1	0	GND		95	95	-
b7_amp2	0	GND	10	50	60	1P
vbase	0	GND	46	50	96	1P

Total Bias failures: 24 (15 bypassed to VDD and 9 bypassed to GND)

Type:

1 : Startup
2 : Standard
1P: Pmos Threshold ref.
1N: Nmos Threshold ref.

Anand Kandasamy
anand@bnl.gov