

CSC On-Chamber Functional Signal Requirements

Kurt Vetter
3/28/00

This is a short note in attempt to surface all of the signals and functionality required on the CSC chamber. At present the data channel architecture consists of a single 20-bit uplink from the Sparsifier to ASMII, and dual 16-bit downlinks from the ASMII to the Sparsifier.

1. Required Single Ended SCA signals (14 total)

These signals will be transmitted over the 20-bit downlink G-Link channel as a subset of the twenty available signal lines.

Signal	Type	Description
WA[7..0]	Input	SCA write addresses
Wclk	Input	SCA write clock ,40MHz
RDclk	Input	SCA read clock, 5-8MHz
G0	Input	SCA channel select
G1	Input	SCA channel select
RD	Input	SCA Read Address strobe. Latches SCA read address.
SD	Input	SCA serial (8-bit) read address

Table 1

2. ASM Parameter Monitoring

It would be desirable to monitor current on both the +5VDC and +3.3VDC supplies, primarily for increased current consumption due to radiation exposure. It may also be beneficial to monitor the board temperature of the ASMII. Both currents and temperature could be digitized and transmitted as a series of three data packets multiplexed into the uplink data stream. These measurements would only need to be transmitted at a very low rate (possibly one or a few times per day?).

Signal	Type	Description
+3.3VDC current sense	Output	12-bit word, transmitted as 16-bit G-Link frame
+5.0VDC current sense	Output	12-bit word, transmitted as 16-bit G-Link frame
Temperature	Output	12-bit word, transmitted as 16-bit G-Link frame

Table 2

3. On-Chamber Electrical Calibration

ASM calibration requires generating a digital ramp and measuring the response. The ramp requirements are 256 steps with 12-bit resolution for each step. A pulse is generated for each step of the ramp with an amplitude determined by the DAC setting. For each step N-samples would be read out k - times.

Each step of the 256 step ramp is loaded into a 12-bit DAC. Each of the 12-bit words could correspond to a single frame of downlink data. The DAC then feeds a PFN (pulse forming network) that pulses the anode wires. These pulses are amplified by the Pre-Amp Shaper and stored in the SCA's for readout. The readout scheme for the calibration data could be the same as that of the SCA data. The process is then repeated for each step of the ramp.

Signal	Type	Description
Calibration Data[11..0]	Input	256 x 12-bit words, loaded via G-Link downlink.
Calibration Data Strobe	Input	Strobe in DAC calibration data.
Start Calibration	Input	Initiates calibration sequence. May be required by on-board G-Link controller.

Table 3

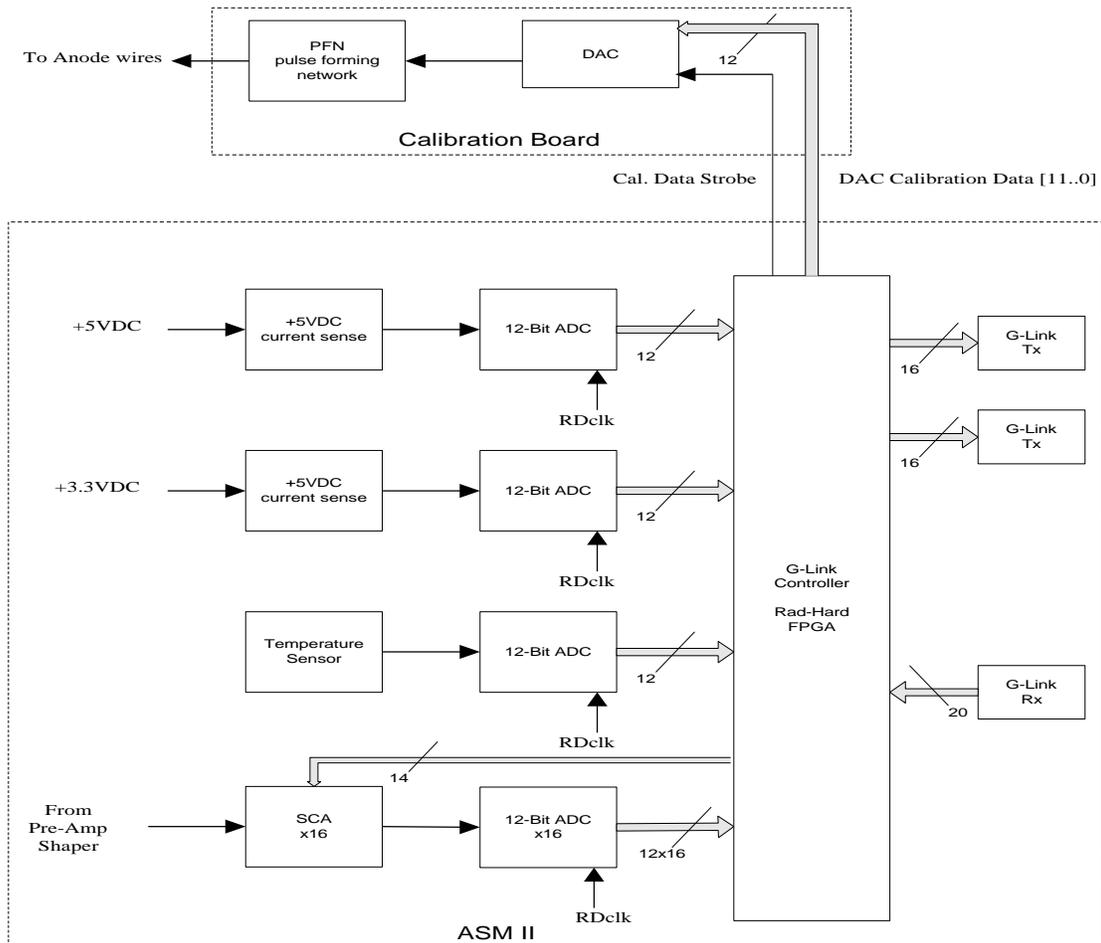


Figure 1. (Integration of SCA data, Calibration and Monitoring)

4. Summary of Uplink Signal Requirements

Signal	Type	Description
WA[7..0]	Input	SCA write addresses
Wclk	Input	SCA write clock ,40MHz
RDclk	Input	SCA read clock, 5-8MHz
G0	Input	SCA channel select
G1	Input	SCA channel select
RD	Input	SCA Read Address strobe. Latches SCA read address.
SD	Input	SCA serial (8-bit) read address
Calibration Data[11..0]	Input	(12-bit x 256 words) loaded via G-Link downlink.
Calibration Data Strobe	Input	Strobe in DAC calibration data.
Start Calibration	Input	Initiates calibration sequence. May be required by on-board G-Link controller.

Table 4

5. Summary of Downlink Signal Requirements

Signal	Type	Description
SCA Data[11..0]	Output	(12-bit x 16words) per sample
+3.3VDC current sense	Output	12-bit word, transmitted as 16-bit G-Link frame
+5.0VDC current sense	Output	12-bit word, transmitted as 16-bit G-Link frame
Temperature	Output	12-bit word, transmitted as 16-bit G-Link frame

Table 5

6. Other Items to Consider

- Is it necessary that each of the ASM boards have a unique address that can be transmitted over the data link?