

G-Link and Gigabit Ethernet Compliant Serializer for LHC Data Transmission

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Abstract

Several LHC detectors require high-speed (\sim Gbit/s) digital optical links for transmission of data between the different sub-detectors and the data acquisition systems. Typically, high-speed data transmission is required for both the trigger systems data path and the data readout systems. In general, those links will be uni-directional with the transmitters located inside the detectors and the receivers situated in the control rooms. In this arrangement, the transmitters will be subject to high radiation doses over the lifetime of the experiments. To address this problem, high-speed radiation hard transmitter IC's were developed in a mainstream sub-micron CMOS technology employing radiation tolerant layout practices. The first prototype developed incorporates the most critical functions of the high-speed transmitter. Its behavior under total dose irradiation as well as its susceptibility to single event upsets was studied and the results are reported here. Based on the experimental data, the behavior of the IC in different LHC environments was extrapolated. Following the experience gained with first prototype, a transmitter IC has been developed that supports both the G-Link and the Gigabit Ethernet protocols for transmission of data in trigger and data readout links. The IC's, their functionality and the experimental results will be described in the paper.

I. SUMMARY

Transmission of high-speed digital data between the LHC high-energy physics detectors and the data acquisition systems require unidirectional links with the transmitters located inside the detectors and the receivers situated in the control rooms. The transmitters must thus be capable of withstanding high radiation doses over the lifetime of the experiments. Additionally, their operation must be robust against Single Event Upsets (SEU) to avoid excessive dead time and transmission errors.

The development of low-cost data links relies heavily on the use of high-volume production devices whenever possible. Components that fall in this category are the receiver IC's that will operate in a non-radioactive environment in the counting rooms and thus are not required to be radiation tolerant. For compatibility with commercial products, any custom made transmitter should support existing communication standards. Along these lines, the developed IC's supports two communication protocols: the G-Link and the Gigabit Ethernet standard. The choice of these two protocols was made with two applications in mind: data trigger links and data readout links. The G-Link protocol, being synchronous, is appropriate for trigger data links since, in this case, data transmission must be synchronized with the LHC system clock, while the Gigabit Ethernet protocol is more convenient for asynchronous data transmission as is often required in data readout links.

A. Serializer prototype

A first prototype of the IC was built that incorporates the most critical functions of the high-speed transmitter such as the high-speed serializer and the clock multiplying PLL [1]. The purpose of this prototype was twofold: to study the feasibility of a high data rate transmitter in low cost main stream CMOS technology and to study the tolerance of the transmitter against high radiation doses and single event upsets.

The block diagram of serializer ASIC is shown in Figure 1. Its operation can be described as follows: an external 20-bit wide bus accepts parallel data at a rate of 60MWords/s. This data is time division multiplexed by the "Word Mux" into two 10-bit words which are then feed to the "10-bit Serializer" at a rate of 120MWords/s. Then, the serializer converts the 10-bit words into an 1.2Gbit/s serial stream. Finally, the data out of the serializer is passed to the "50 Ω Output Driver" that converts the internal CMOS levels into Pseudo-ECL (PECL) levels to allow interfacing the ASIC with commercial optical transmitters. The operation requires several clocks and control signals at different frequencies. These are generated in the IC by the Phase-Locked-Loop (PLL) and the "Clock Generator" circuit. For operation at 1.2Gbit/s, the PLL takes as its reference the 40.08MHz LHC clock and compares it with its output

signal divided by the "Clock Generator" by a factor of 30. In this way, a 1.2GHz clock is obtained at the PLL output. The "Clock Generator" provides the 60 and 120MHz clock signals required by the "Word Multiplexer", the 600MHz clock and the "load" signal needed by the high-speed serializer. A detailed description of the circuit and its operation can be found in [1].

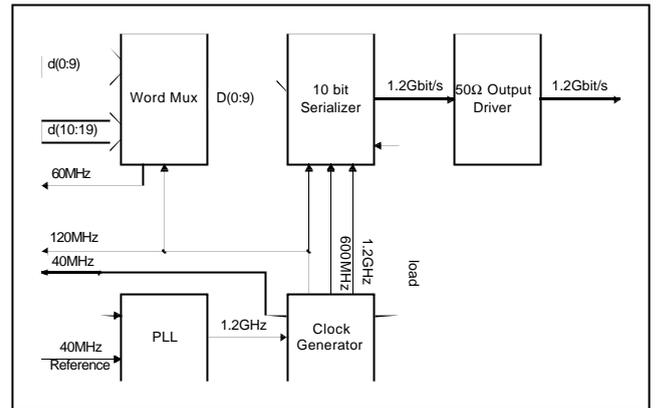


Figure 1 1.25Gbit/s serializer ASIC block diagram.

A bit error rate test-setup has been developed for the serializer ASIC. At the receiver end of the test-setup a commercial G-Link receiver is used to de-serialize the incoming data and to check for transmission errors. The tests proved the ASIC prototypes to be fully operational at 1.2Gbit/s data rate. The data transmission test was done both before and after irradiation with X-rays. In both cases the data link was operated error free for several days. The irradiation was performed in a single step to a total dose of 10Mrad (SiO_2) at a dose rate of 11.7Krad (SiO_2)/min. The post-irradiation data transmission test was initiated one hour after irradiation. Jitter measurements were made before and immediately after irradiation to evaluate any possible degradation of the analogue performance of the circuit. The jitter was measured with an HP infinium oscilloscope having a 1.5GHz analog bandwidth and a time resolution of 8Gs/s. The measured jitter values are 22ps RMS and 170ps PP, that are essentially the numbers obtained for the pre-irradiation measurements.

The circuit sensitivity to Single Event Upsets (SEU) was studied by irradiating the IC with heavy ions while monitoring the transmitted data for errors. In this experiment it was verified that the main cause of transmission errors was loss of synchronization between the transmitter and the receiver. The measured cross-section for loss of synchronization is plotted in Figure 2 as function of the Linear Energy Transfer (LET) of the ions. The observed threshold is about 7Mev cm^2/mg and the saturation cross-section is $4 \cdot 10^{-5} \text{cm}^2$ (no errors were observed for LET = 6.2Mev cm^2/mg , fluence $9 \cdot 10^6$). Using the measured data and extrapolating for different LHC environments, as proposed in [2], the error rates for such device can be estimated. This is done in Table 1 where four different

CMS environments are considered. The numbers given in the table were calculated assuming a sensitive volume of $1 \mu\text{m}^3$.

Table 1 Error rates per chip per hour in for different CMS environments

Environment	Pixel R = 4-20cm	Endcap ECAL R = 50-130cm	Outer Tracker R = 65-120cm	Expt. Cavern R = 700-1200cm
Errors/(chip hour)	$1.4 \cdot 10^{-2}$	$1.9 \cdot 10^{-4}$	$8.4 \cdot 10^{-5}$	$3.1 \cdot 10^{-8}$

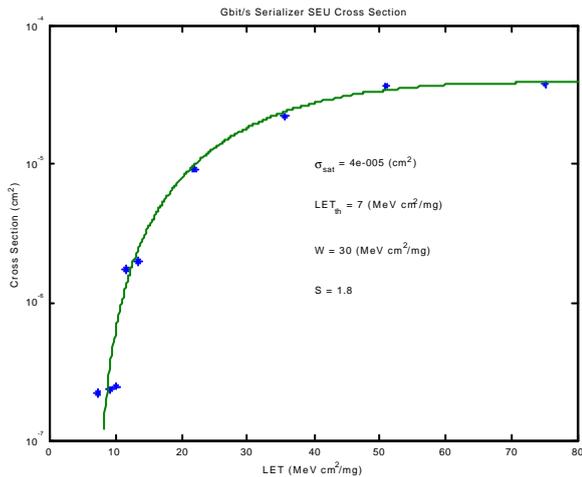


Figure 2 Experimental cross-section

B. G-Link and Gigabit-Ethernet compliant serializer

A transmitter IC that is compliant with both the G-Link and the Gigabit Ethernet has now been developed. In the G-Link compatible mode data is transmitted synchronously with the LHC clock, that is, each LHC clock cycle a user word is transmitted with fixed latency. In the G-Link mode two user word sizes are allowed, 16 and 24bit wide words, resulting in 640 and 960Mbit/s user data rates. In the Gigabit Ethernet mode the user can choose between 16 and 32bit wide words, corresponding to 640 and 1280Mbit/s user bandwidths. In this mode the ASIC operates in an asynchronous mode, that is, the user first fills an internal FIFO with the data stream to be transmitted and only after a send strobe from the user is the data transmitted. Before transmission, the receiver embeds the user data in a Gigabit Ethernet compliant frame.

Experimental results for this prototype are expected to be available by the time of the conference.

II. REFERENCES

- [1] P. Moreira et al, "A 1.25Gbit/s Serializer for LHC Data and Trigger Optical Links", *Proceedings of the Fifth Workshop on Electronics for LHC Experiments*, Snowmass, Colorado, USA, 20-24 September 1999, pp. 194-198

- [2] M. Huhtinen and F. Faccio, "Computational method to estimate Single Event Upset rates in an accelerator environment", To be published by Elsevier