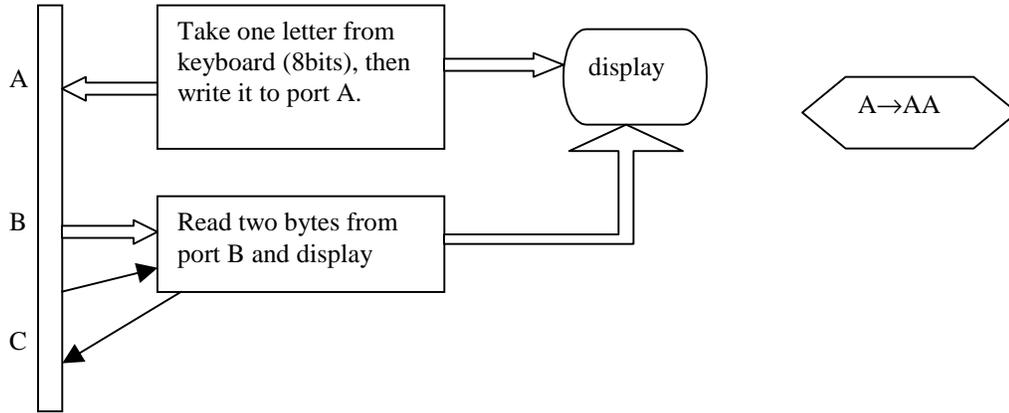
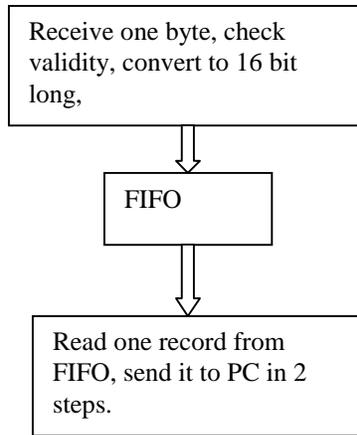


FPGA & PC communication test plan

PC: NI-DAQ interface, Port A (8bits) write to FPGA
 Port B (8bits) read from FPGA
 Port C, utilize 2 lines, one for flag, one to acknowledge read



FPGA:



Simple full functionality test plan(little change to the existing Verilog code)

