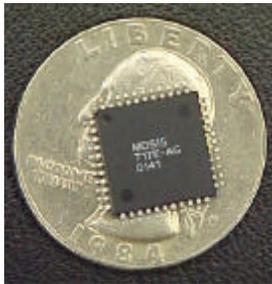


ASM2 MULTIPLEXOR

Features:

- +3.3V Power supply
- Low Power Dissipation (< 20 mW)
- 40 MHz Write Clock
- 6.6667MHz or 5 MHz Read Clock
- Long Input Data Propagation Delay
- 16mA Output current capable drivers

General Description:



The ASM2¹ Multiplexor (ASM2MUX) Application Specific Integrated Circuit (ASIC) is designed for the ATLAS MUON Cathode Strip Chambers (CSC). This multiplexor is intended for multiplexing 192 bits of Analog-to-Digital converter (ADC) data from sixteen 12-bit ADC's² into Agilent Technologies Physical Layer Transmitter IC for Gigabit Links (HDMP-1024).

Each ASM2MUX accepts 12-bit digital word from two ADC's and outputs them into a 4-bit output word. It takes 6 write clock cycles to multiplex out all 24 bits of ADC data.

The ASM2MUX is fabricated in Hewlett Packard 0.5micron Triple-Metal 3.3V CMOS process (HP AMOS14TB) and packaged in 44-pin plastic thin quad flat pack (TQFP).

Layout:

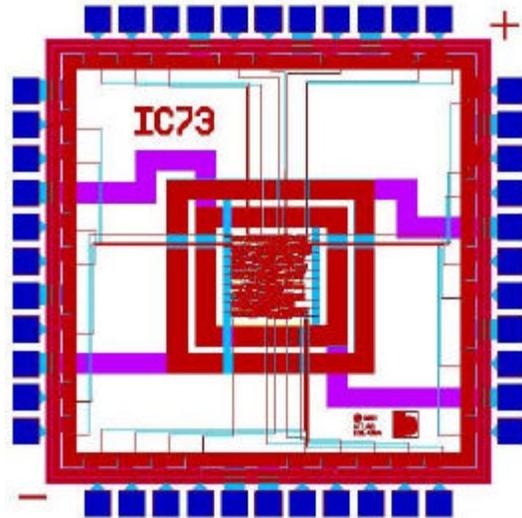


Figure 1. Die Metalization Photograph

Die Size: 2.22mm x 2.22mm

Total Transistors: 1744

Package:

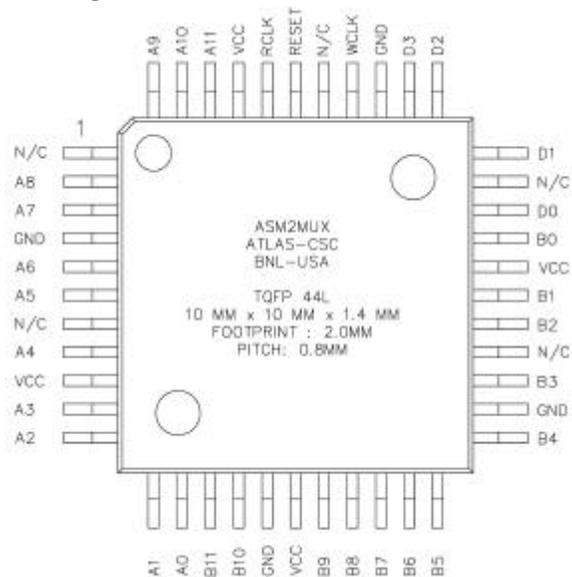


Figure 2. Package and Pin-out

44-pin Plastic TQFP package and Device pin-out is shown in Figure 2.

ASM2 MULTIPLEXOR

Pin Description:

Pin Names	Description
A11-A0	12-bit digital input word 1
B11-B0	12-bit digital input word 2
D3-D0	4-bit digital output word
RCLK	Read clock (ADC sampling clock) 6.6667MHz/5.0MHz
WCLK	Gigabit-Link transmitter clock, 40 MHz
RESET	Active Low reset input
VCC	Power, +3.3 Volts
GND	Power, 0 Volts
N/C	Not/Connected

ASM2MUX – Specifications:

Test Conditions:

VCC: +3.3V

GND: 0V

Output Load: 10K Ω and 20pF

Temperature: 25° C

Parameters		
Read Clock	(a)	6.6667 MHz
	(b)	5.0 MHz
Write Clock		40 MHz
Setup Time	T _S	< 1 ns
Hold Time	T _H	< 1 ns
Output Propagation Delay	T _D	3.6 ns
Output Rise Time	T _R	1.27 nS
Output Fall Time	T _F	837 pS
Output drive current	I _{out}	16 mA (max)
Power	I _{VDD}	6.0 mA

(a) WCLK/6; (B) WCLK/8

Functional Description:

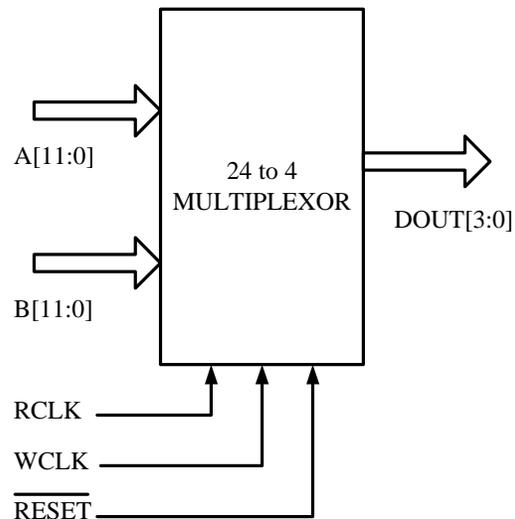


Figure 3. Functional Diagram

As shown in Figure 3, ASM2MUX device has two 12-bit digital inputs and one 4-bit digital output. The device requires two clocks namely RCLK and WCLK. The device also has an active low reset input. For all practical purposes this pin can be tied to VCC for normal operation.

The device requires 6-cycles of its 40 MHz write clock to slice and output its 24 inputs into 4 bit output words. The output bit sequence from the device is shown in Figure 4.

The read clock (RCLK) to the device is the same 6.6667 MHz clock that is used for the ADC sampling clock in the CSC system board namely ASM2. The device can also be operated with a read clock of 5 MHz. In the 5 MHz mode of operation there will two empty 40 MHz output clock cycles during which the data from the device can be ignored.

ASM2 MULTIPLEXOR

Output Bit Sequence:

Input A	A11-A8	A7-A4	A3-A0
Input B	B11-B8	B7-B4	B3-B0
CLK 1	A3-A0		
CLK 2	A7-A4		
CLK 3	A11-A8		
CLK 4	B3-B0		
CLK 5	B7-B4		
CLK 6	B11-B8		

Figure 4. Output Bit Sequence

To understand the operation of this device better a functional block diagram of a section of the system in which the device will be used is shown in figure.

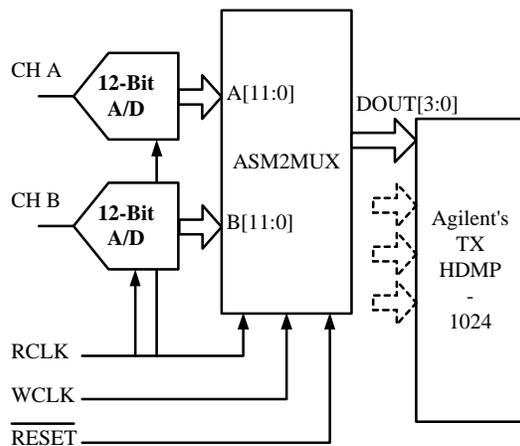


Figure 5. ASM2MUX System block diagram

Each ASM2MUX accepts outputs from two 12-bit ADC's. These ADC's sampling clock and ASM2MUX's read clock are the same (RCLK). The 4-bit output word of the ASM2MUX is connected to the 4 input bits out of 16

bits of the Agilent Technologies Transmitter Chip. The remainder of the 12-bits for this transmitter comes from three more ASM2MUX devices.

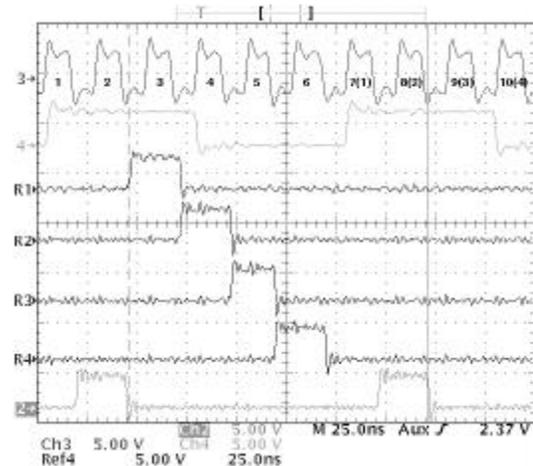


Figure 6. Timing Diagram

The timing diagram for the device is shown in Figure 6. The first signal (3) is the 40 MHz write clock. Signal 4 is the 6.6667 MHz read clock. During the rising edge of the read clock the data from the ADC is available at the inputs of the ASM2MUX after a 9 ns propagation delay³. This data is latched on to the input latches of the ASM2MUX on the rising edge of the wclk #2. The internal muxing sequence starts at the rising edge of wclk#2 and takes 6 cycles to complete from wclk#2 to wclk#7. The output from the device is available during the negative edge of its respective internal multiplexor selection cycle as it can be seen from Figure 6. This is done so that enough timing margin exists for the gigabit link chip to serialize the output data from the ASM2MUX devices. The gigabit link latches its inputs on the rising edge of the write clock. So, the ASM2MUX device has a 2.5 write clock cycle latency at its output and the data output

ASM2 MULTIPLEXOR

stream coming out of the gigabit link chip has a 3 write clock cycle latency.

The timing diagram also shows one of the output bits (bit DOUT0) for its 6 output cycles (cycle #5 is left out for clarity). Waveform R1 is input bit A0, R2 is input bit A4, R3 is input bit A8, R4 is input bit B0 and Waveform 2 is input bit B8.

Input and Output Waveform:

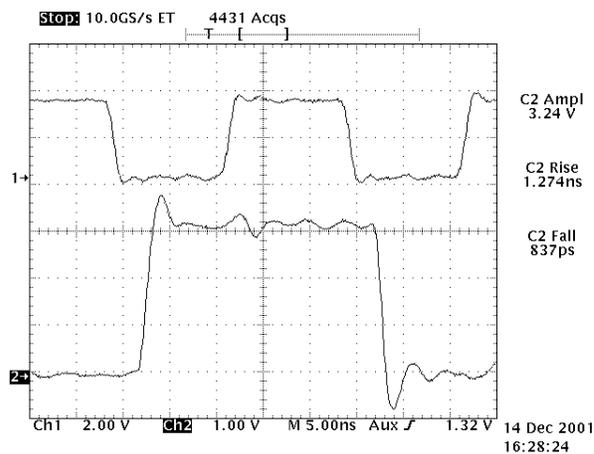


Figure 7. Output Timing

Channel 1: Write clock
Channel 2: Output Data (Bit D0)

As shown in Figure 7, the output is available on the negative edge of the write clock after a propagation delay of 3.6ns. Also it is clear that there is enough timing margin for the rising edge of the write clock to latch this data into the input latches of the gigabit link transmitter chip.

The input data is latched into the input latches only on the rising edge of write clock cycle #2 (refer to Figure 6). This gives the ASM2MUX the capability to work with ADC's with longer output

propagation delay. This delay can be up to a maximum of 24ns. (write clock period less the setup time of the input latches). The input timing is illustrated in

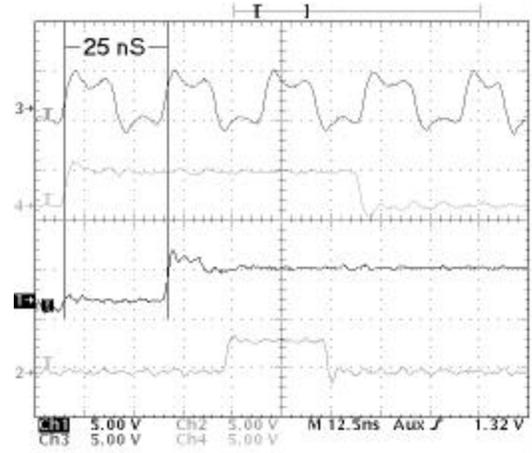


Figure 8. Input Timing

Channel 1: Input Data (Bit A0)
Channel 2: Output Data (Bit D0)
Channel 3: Write Clock
Channel 4: Read Clock

Testing:

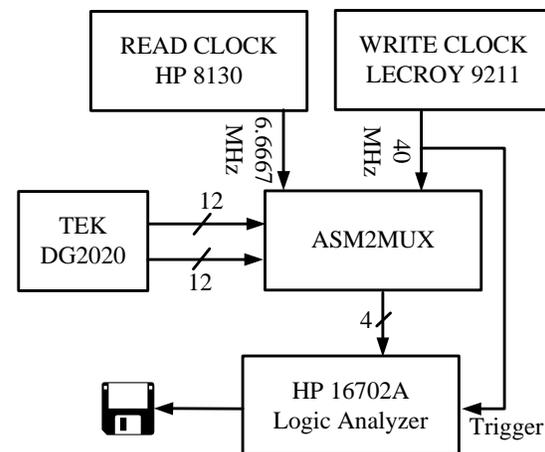


Figure 9. Test Setup

The test setup consisted of the basic components as shown in Figure 9. The input data was generated using Tektronix Data Generator DG2020. One

ASM2 MULTIPLEXOR

of the output pod was configured to count up 12 bits and the other was configured to count down 12 bits. The output 4 bit data was collected using HP 16702 Logic analyzer running as a state machine triggered by the write clock. Each acquisition stored 2M samples, having at least eighty 4096 count up/down cycles. The acquired data was stored to an ASCII formatted file. A perl script was written to format the raw data file and reconstruct the 12 bit input digital word. The program also compares the output with the expected output and flags mismatches.

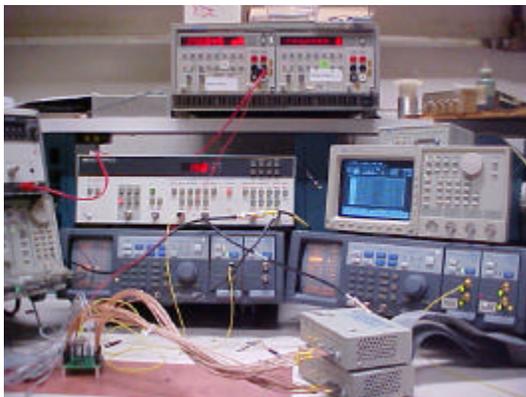


Figure 10. Test Bench

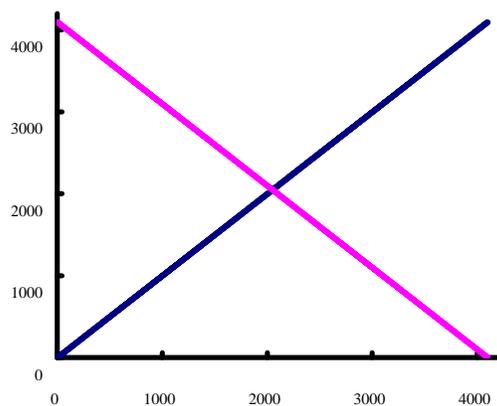


Figure 11. Reconstructed output code
X-Axis: Sequence Num.; Y-Axis: Code

Figure 11 illustrates the reconstructed input data. Y axis represents the reconstructed code and the X axis represents the sequence order. It can be seen the output data being reconstructed correctly to match the 12-bit up count and 12-bit down count.

The test board used in these tests are shown in Figure 12

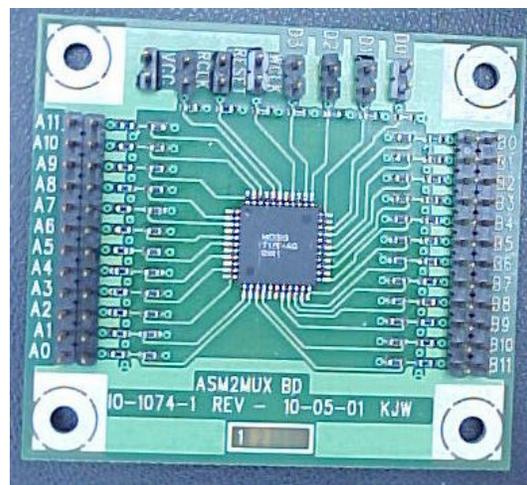
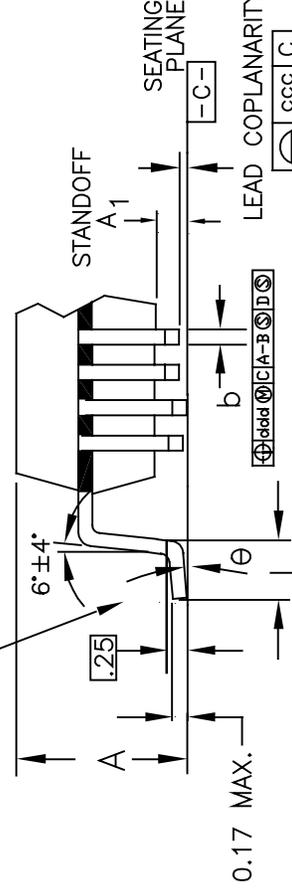
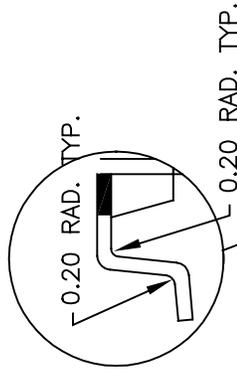
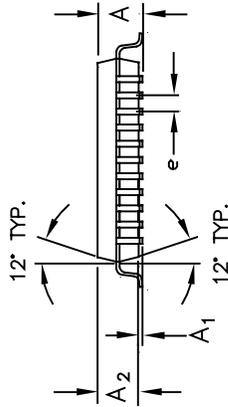
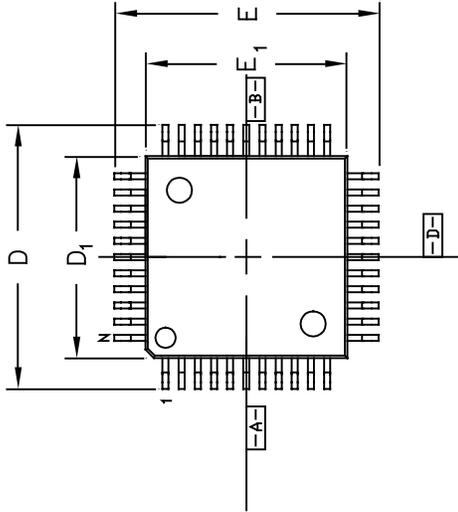
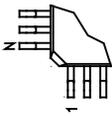


Figure 12. Test Board



ANOTHER VARIATION OF PIN 1 VISUAL AID



REVISIONS

ECN	REV	DESCRIPTION	DATE	APPROVED
HK5644	A	CHANGE D & E TOL. TO ±.20, NEW DRAWING	5/16/95	

PACKAGE THICKNESS		BODY + 2.00 mm			
DIMS.	TOL.	44L	64L	52L	64L
A	LEADS	1.20	1.20	1.60	1.60
A1	MAX.	.05 MIN./ .15 MAX.			
A2		1.00		1.40	
D		±.05		12.00	
D1		±.10		10.00	
E		±.20		12.00	
E1		±.10		10.00	
L		+.15/- .10			
e	BASIC	.80	.50	.80	.65
b		±.05	.22	.35	.30
θ		0°-7°			
ddd	MAX.	.20	.13	.08	.20
ccc	MAX.	.10	.08	.10	.08

NOTES: 1) ALL DIMENSIONS IN MM.

2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED.

3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") OR 0.15 MM (.006") THICK.

4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.

DRAWN		ASAT Inc.	
AHSAN		10x10 mm TQFP	
DATE		MARKETING OUTLINE	
5/3/95			
CHECKED	DRVG NO:	REV	SHEET
NIC B.	DGMF 10101	A	1/1

¹ ASM: Amplifier Storage Module.

² 192 Bits for the each system board. Each ASM2MUX handles 24 bits of ADC data requiring 8 ASM2MUX for each system board.

³ Refer to Analog Devices AD9042 Data sheet.