PRODUCTION READINESS REVIEW REPORT

CSC Electronics

Abstract

The PRR of the CSC electronics was held at CERN on June 24th 2004. This document gives the report of the review.

Prepared by :	*Checked by :*	*Approved by :*
Ph. Farthouat Cern	**Francis Anghinolfi, Cern** **Georges Blanchot, Cern** **Robert McLaren, Cern** **Robert Richter, MPI**	**M. Nessi**

for information, you can contact :	**Ph. Farthouat**	Tel. +41.22.767 6221	Fax. +41.22.767 8350	E-Mail Philippe.Farthouat @cern.ch

Distribution: EB Members, CSC Members, all participants mentioned in the report.

PURPOSE OF THIS REVIEW

The purpose of the review was to give the green light for the production of the CSC electronics.

MEMBERS OF THE REVIEW COMMITTEE

Review Committee

F. Anghinolfi, Cern
G. Blanchot, Cern
Ph. Farthouat, Cern
R. McLaren,Cern
R. Richter, MPI

CSC Team

A. Lankford, Irvine
S. Junnarkar, BNL
A. Kandasamy, BNL
P. O'Connor, BNL
S. Pier, Irvine
V. Polychronakos, BNL

Ex officio

M. Nessi, CERN
G. Mikenberg, Weizman

For Information

AGENDA & DOCUMENTATION

The agenda and documentation are available at

http://agenda.cern.ch/fullAgenda.php?ida=a042614

OUTCOMES

ASM1 and ASM2
The design is mature and well understood and several prototypes have been used over the past years.

Nevis confirmed that the components purchased and used by the Liquid Argon Electronics and by the CSC Electronics, namely the MC10H116, AD8042, AD9042, have been effectively qualified for radiation level above the worst case represented by the CSC location:

MC10H116	5E13 neutrons.cm-2	3.4Mrads
AD9042	2E13 neutrons.cm-2	1Mrad
AD8042	4E13 neutrons.cm-2	2.7Mrads

The cooling system design is sound.

Grounding scheme
The design of the chambers in form of faraday cage, the use of grounding strips to provide ground mesh, and the use of linear regulators on the chamber provide insures the proper performance of the system. However and in order to comply with the CERN electrical code and with the ATLAS EMC policy, the chambers shall additionally be grounded to the safety ground. A grounding scheme which includes this connection must be sent to G. Blanchot.

LV and HV distribution
The power is distributed by means of unshielded cables. The performance observed at the testbeam

is sufficient; however, and despite the fact that there are local voltage regulators, the system is exposed to EM fields in the experimental area that can turn into common mode noise. The use of shielded cables, with the shield bonded to the faraday cage and to the power supply front panel, would protect the LV cables against EM fields and provides a low inductive return path for common mode currents, therefore reducing the radiated emissions. If affordable and practical, it should be considered to use shielded cables.

The conducted noise through the LV and HV cables, and the immunity to CM noise, must be measured according to the ATLAS EMC procedures.

ROD

For the ROD part of the review, the reviewers felt that the design fulfilled the requirements of the FDR but failed to achieve the level of maturity demanded by a PPR. In order to reach the required level, more work is needed in the system test area. A complete slice of the system (ASMs, TMs, CRB, ROD, Tim and RCC) should be built and run at full rate.

A document outlining the testing methodology for the production units should be drafted. Complete documentation should be entered in EDMS (see for instance https://edms.cern.ch/cedar/plsql/navigation.tree?cookie=2845106&p_top_id=1579370442&p_top_type=P&p_open_id=1477290025&p_open_type=I).

The board operates at different frequencies up to 800MHz, with rise and fall times as fast as 0.5nsec, and with traces up to 1 meter long. Under these conditions, and even if the signal integrity simulation for a single board looks fine, the traces will behave as EM radiators that can couple interferences to neighbouring boards of the crate. For these traces, it is strongly recommended to at least serial terminate the lines to minimize emissions due to reflections.

It must be noted as well that in case of EMI couplings, the proposed workaround (reduce clock speed) wouldn't help, because it is the rise and fall times that define the spectrum width of radiated emissions. The workarounds shall include the possibility to slow down the rise and fall times of the signals.

A system test, including at least two ROD boards in the crate, must be carried on in order to test the level of immunity to radiated noise.

RECOMMENDATIONS

The production process of the front-end board can start. A follow-up review for the ROD should be organised after the full slice system test has been done.