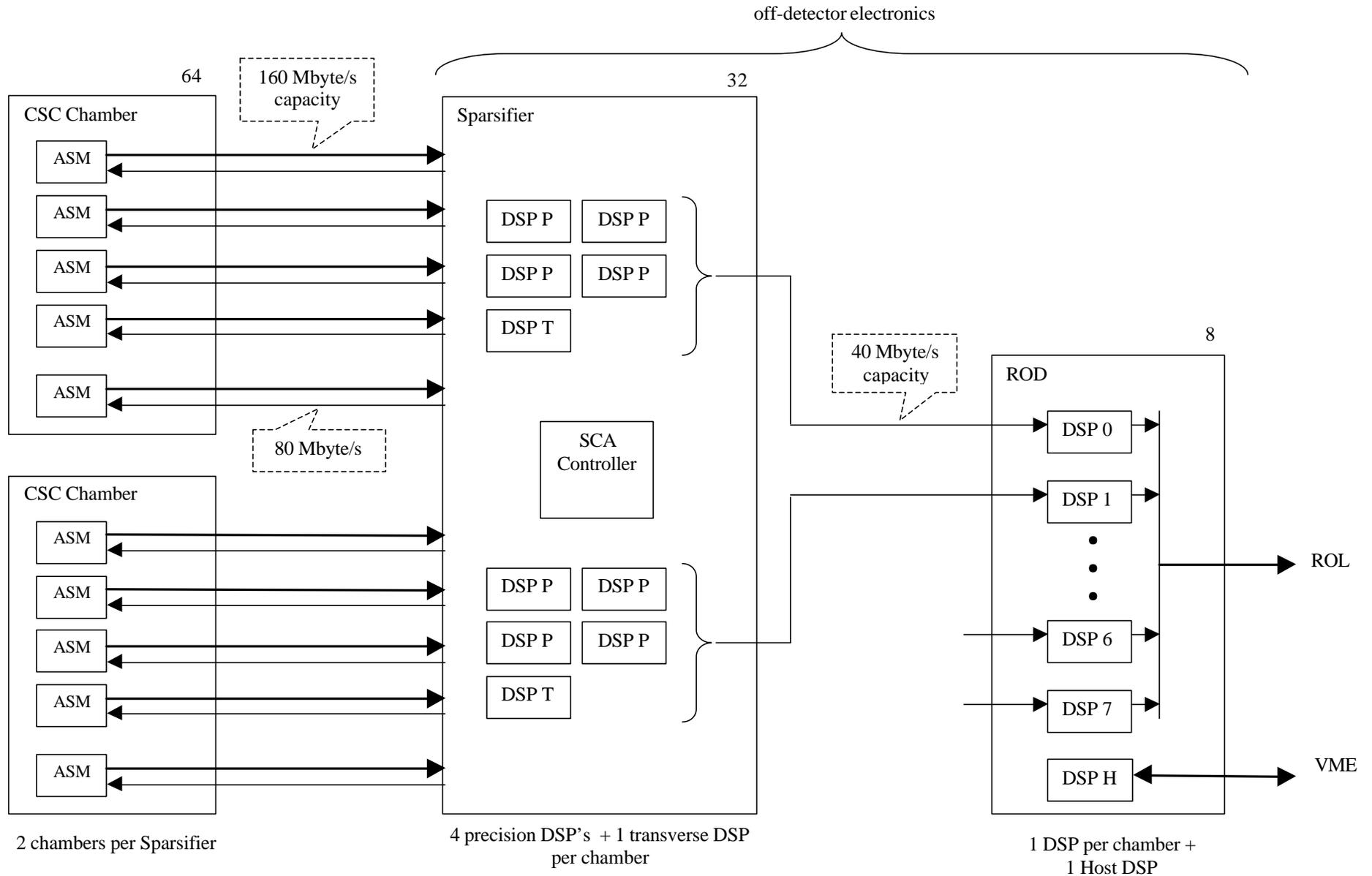
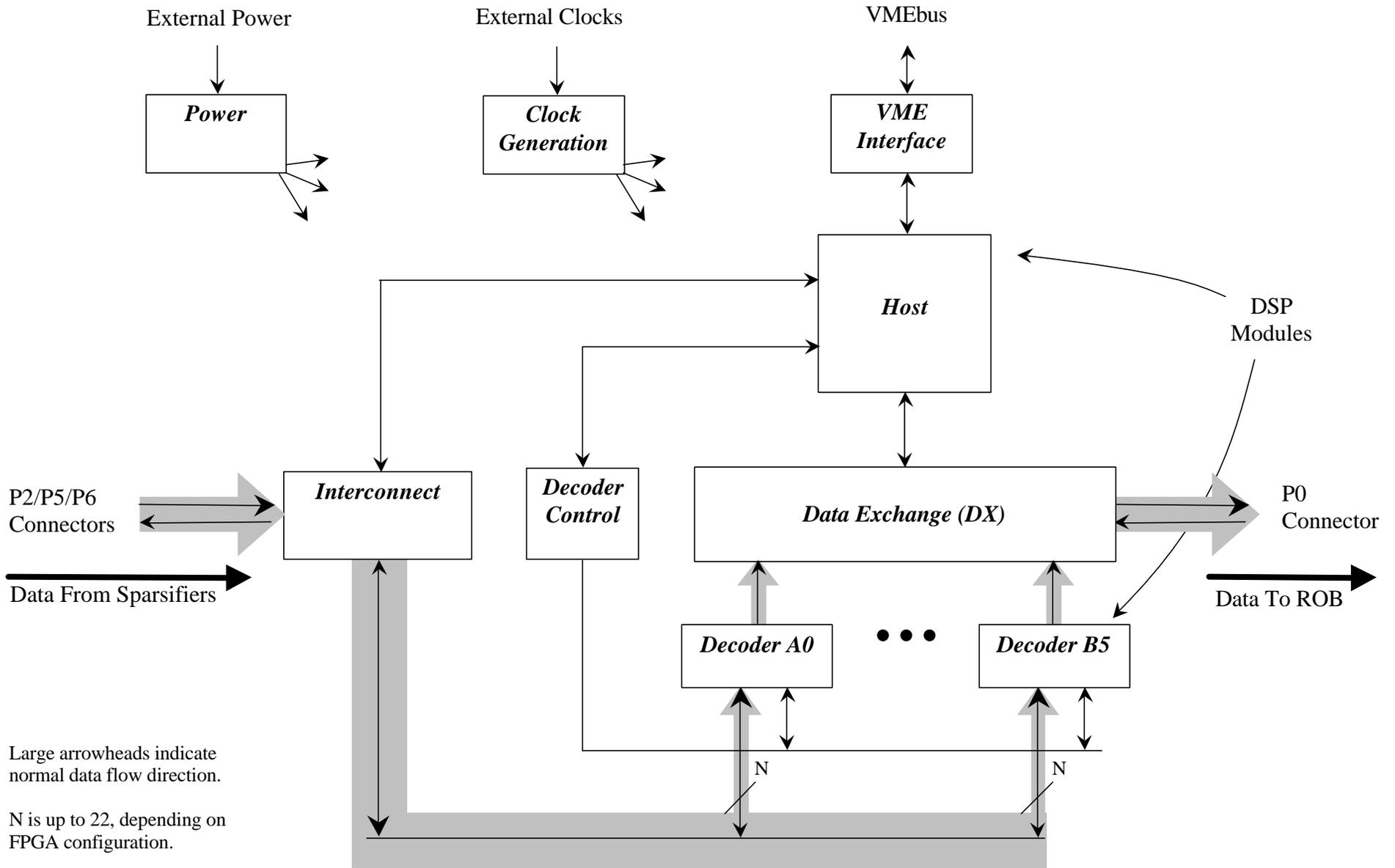
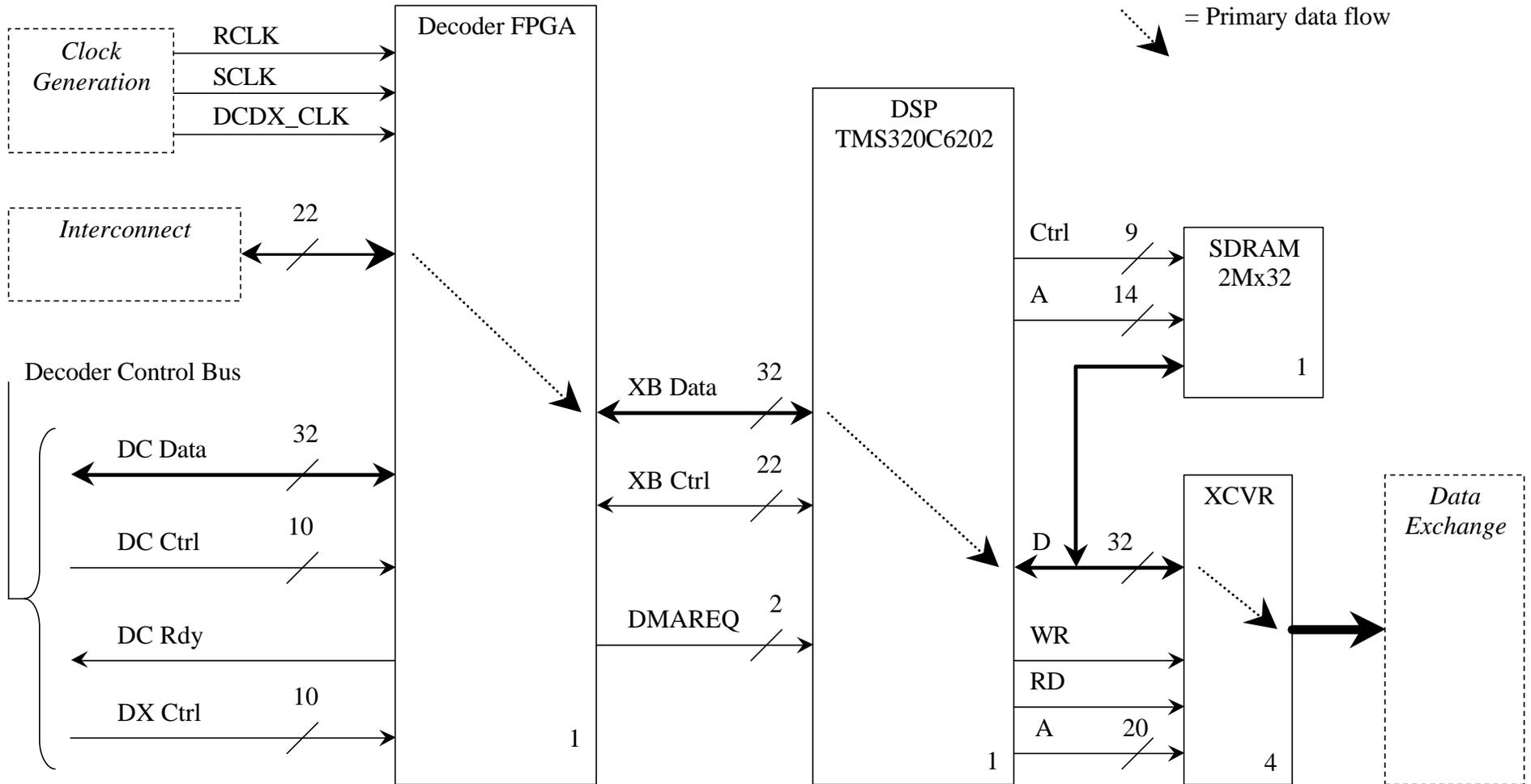


# **CSC Readout Electronics Overview**





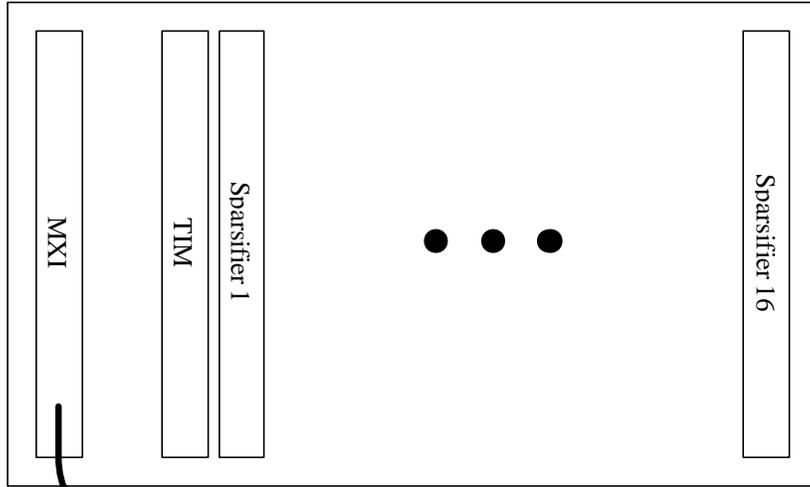
# Decoder (= DSP Module)



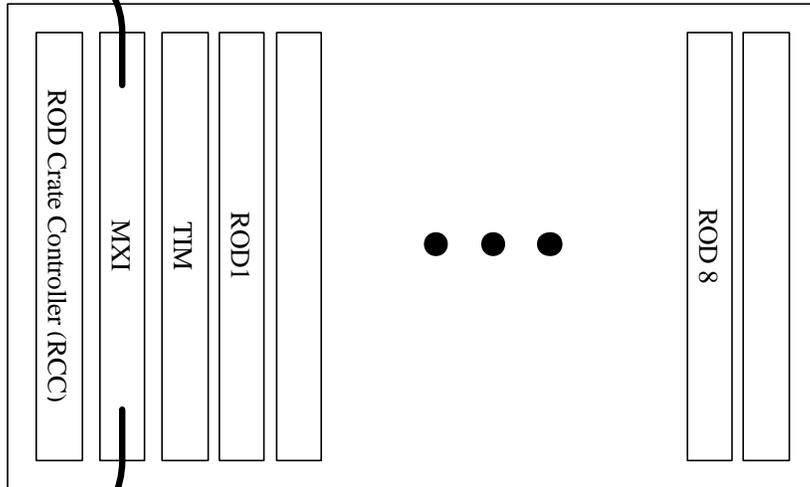


# CSC Off-Detector Electronics Crates (Front View of Rack)

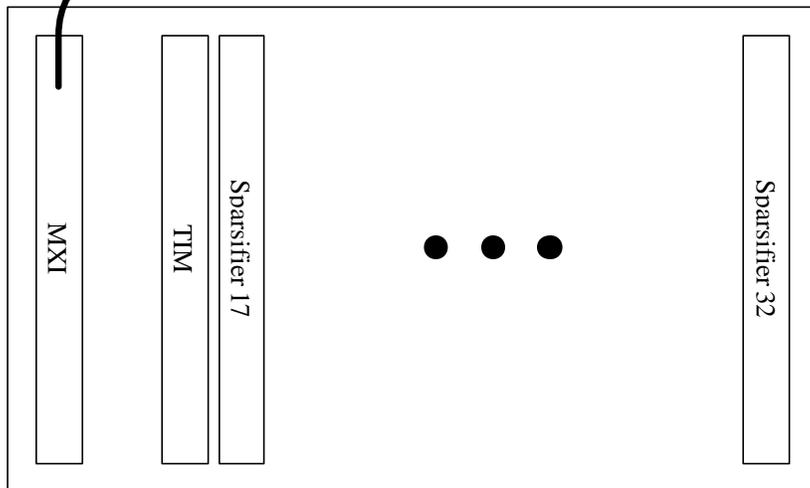
Sparsifier Crate 1



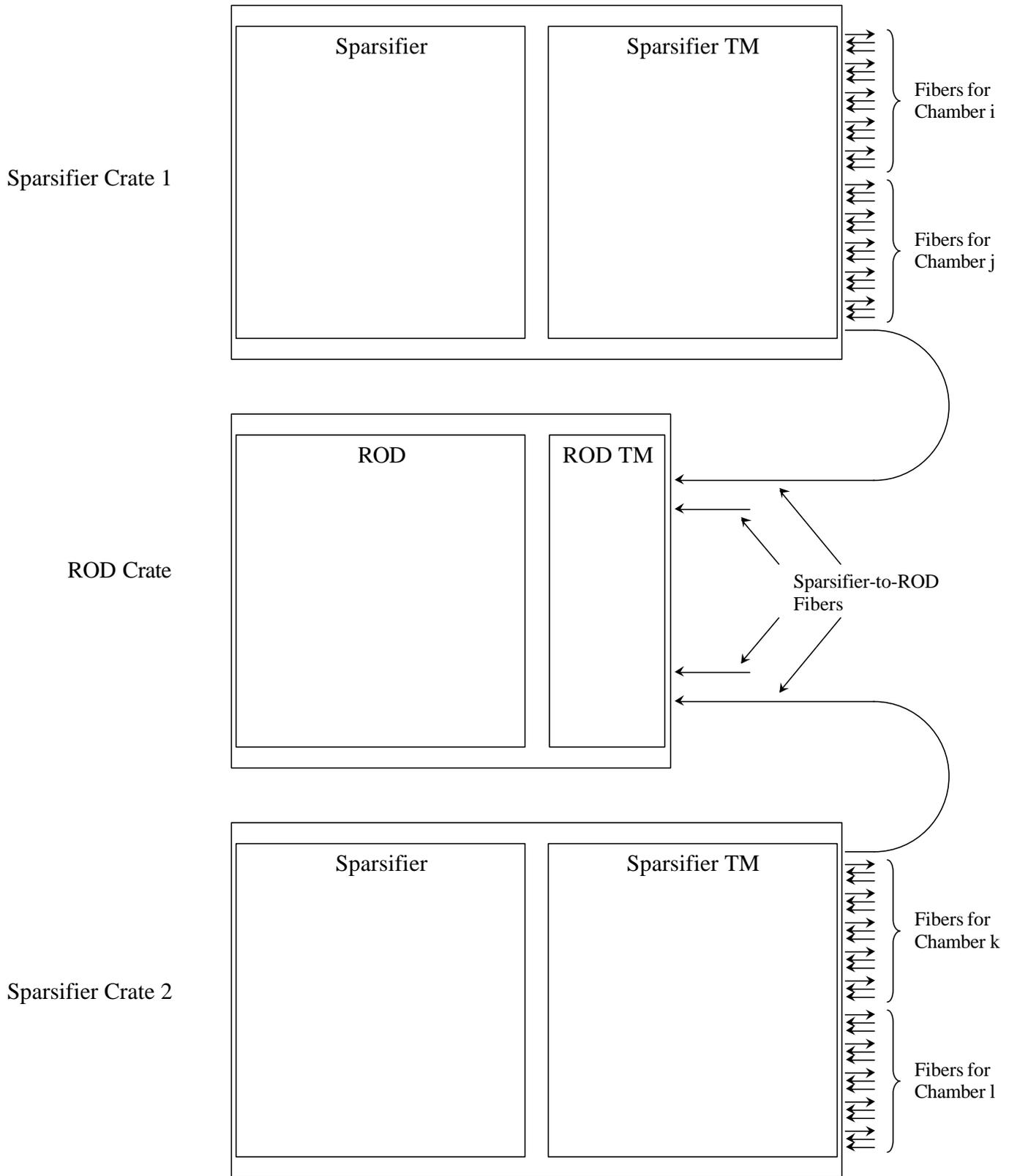
ROD Crate



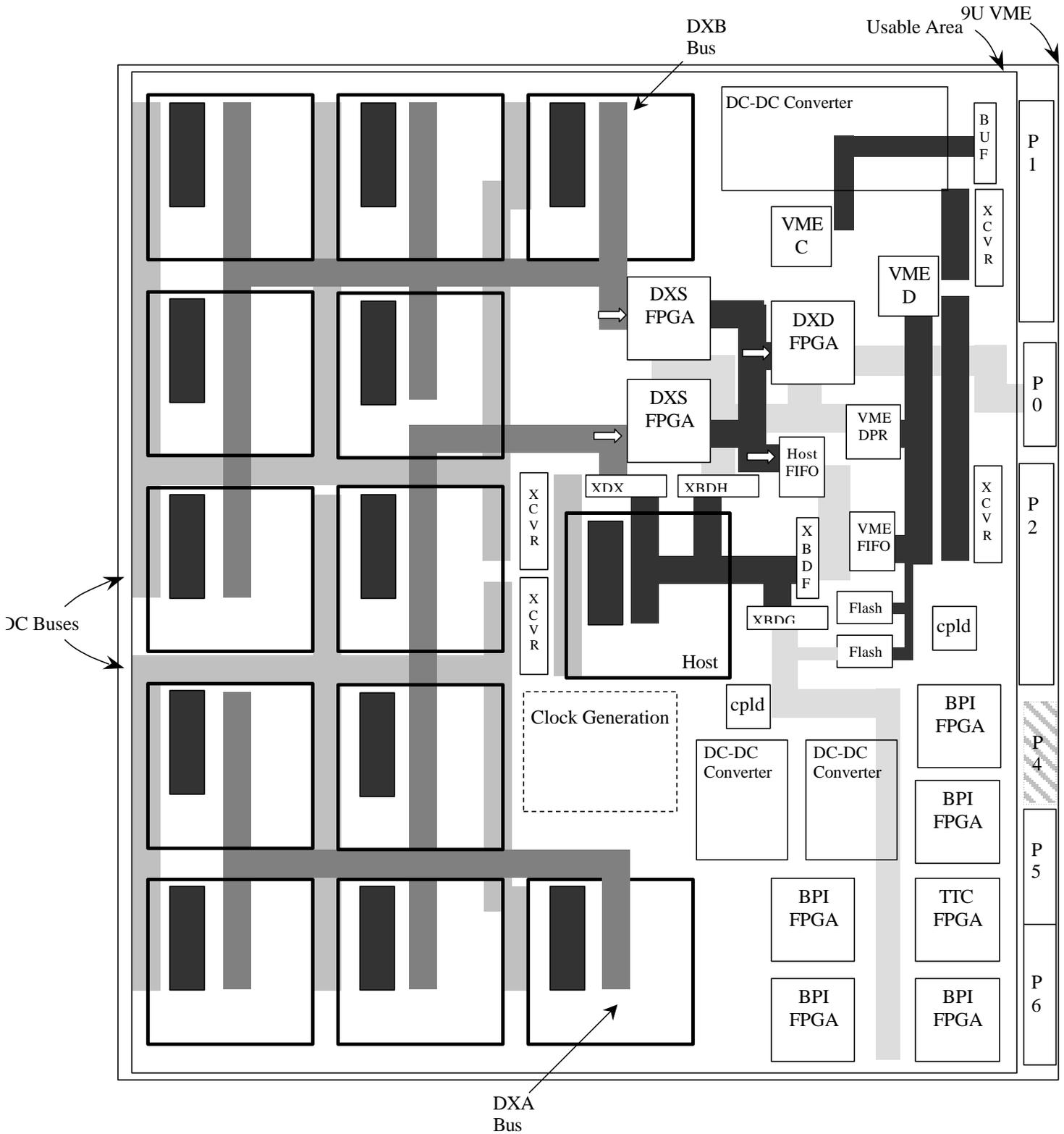
Sparsifier Crate 2



# Example Transition Modules (Side View of Rack)



# ROD/Sparsifier Layout



DX = Data Exchange  
 DC = Decoder Control  
 BPI = Backplane Interface

## 1. Sparsifiers

- Accept digitized chamber data sent via optical G-Link (6.4 Gbit/s per chamber max).
- Check, sparsify, reformat chamber data.
- Transmit sparsified data to ROD.
- Generate all control signals needed on-chamber, including SCA control.
- Transmit control signals and beam clock to chambers via optical G-Link.
- Much former on-chamber functionality now resides in the Sparsifiers.
- 9U boards, 32 boards service 64 chambers.

## 2. Readout Drivers

- Accept sparsified data from Sparsifiers.
- Check sparsified data, apply calibration constants, reject neutrons (optional).
- Build ATLAS standard events by gathering data from eight chambers.
- Transmit events to Readout Buffer (ROB) via Readout Link (ROL).
- Monitor data, e.g., count errors, maintain statistics, fill histograms, etc.
- Perform non-runtime functions such as system initialization and calibration runs.
- 9U boards, 8 boards service 64 chambers.

## 3. Support Electronics

- Physically support and supply power to Sparsifiers and ROD's.
- Interface CSC system to LHC and L1 timing via Timing Interface Module (TIM).
- Interface CSC system to ATLAS Trigger/DAQ, DCS, etc. via Ethernet.
- 3 9U VME crates with custom J5/J6 backplanes.
- ROD VME crate contains one RCC, one TIM, and eight ROD's.
- Each Sparsifier VME crate contains one TIM and 16 Sparsifiers.
- MXI boards in all crates present RCC with one unified VMEbus memory space.

## 4. Software

- Sparsifier Software runs in Sparsifier DSP's (on Sparsifiers).
- Decoder Software runs in Decoder DSP's (on ROD's).
- Host Software runs in Host DSP's (on ROD's and/or Sparsifiers).
- RCC Software runs in Rod Crate Controller (in ROD Crate).

Details posted at: <http://positron.ps.uci.edu/~pier/csc/CSCElectronics.html>

### 1. Sparsifier:

- zero-suppression
- out-of-time hit suppression
- formatting
- event fragment building
- handling of anomalous conditions
- front-end control and buffer management

### 2. ROD:

- applying calibration constants
- out-of-time hit suppression
- neutron rejection
- formatting
- event fragment building
- handling of anomalous conditions
- data monitoring
- histogramming
- calibration control and processing
- sparsifier initialization and control

### 3. ROD Crate Controller:

- messaging with ROD
- ROD initialization and control
- data monitoring
- calibration monitoring
- event sampling
- interface to standard ATLAS RODdaq support

### 1. Sparsifier:

- algorithms studied with Monte Carlo and beam test data
- performance of real-time software studied
- hardware architecture under development
- ROD hardware may be adapted for use as Sparsifier hardware

### 2. ROD:

- architecture stable, implementation in progress
- Verilog coding for FPGA's and CPLD's in progress
- DSP module layout complete (Spartan FPGA)
- DSP module layout being modified for Spartan II FPGA
- performance of real-time software studied
- prototype of motherboard and DSP modules expected in autumn 2000

### 3. ROD Crate Controller:

- software being studied

## Supporting Text

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### CSC Readout Electronics Overview

In order to reduce radiation tolerance issues for on-chamber electronics, the off-chamber electronics for the CSC's must receive the full rate of chamber data:

$$960 \text{ chan/chamber} * 4 \text{ sample/chan/trig} * 12 \text{ bit/sample} * 100 \text{ k trig/s} = 4.6 \text{ Gbit/s/chamber.}$$

Off-chamber electronics must also provide all required readout control signals (SCA read/write addresses, etc.).

Control is transmitted on five gigabit per second fibers per chamber and data is received on five (or five pairs) of gigabit per second fibers per chamber (for each of 64 chambers).

The off-chamber electronics will consist of two module types: the Sparsifier and the ROD.

The Sparsifier generates and transmits the readout and control signals. It also receives the raw chamber data, suppresses channels with no hits, suppresses hits that are out of time, and builds an event fragment for the chamber.

The ROD builds the event fragments received from the Sparsifier into event records that are output on Readout Links (ROL's). It also provides calibration and monitoring capabilities, as well as the capability to perform further preprocessing, such as suppression of neutron hits and further suppression of out of time hits.

The system consists of 32 Sparsifier modules, each supporting 2 chambers, and 8 ROD modules, each supporting 8 chambers.

Recent studies indicate that a dedicated Sparsifier design may be unnecessary. With appropriate firmware and software modifications, a ROD module may be able to function as a Sparsifier. If so, the system would still require 32 Sparsifiers modules and 8 ROD modules, but these modules would all be identical hardware.

The ROD will be prototyped first, with the first full prototype scheduled for Autumn 2000. The ROD prototype can also function as a Sparsifier prototype.

System details are available at:

<http://positron.ps.uci.edu/~pier/csc/CSCElectronics.html>

Note: ROD documentation shows 13 DSP modules per ROD. A CSC ROD needs only 9 DSP modules installed, one per chamber plus one host. A Sparsifier needs 11 DSP modules installed, one per ASM plus one host.

### CSC ROD Subsystems

This is the first page of the ROD architecture block diagram. The full diagram is available at:

<http://positron.ps.uci.edu/~pier/csc/IRODBlockDiagram4.pdf>

The ROD is divided into subsystems, each of which is shown in the diagram and described below:

**Power.** Several power supply voltages are required by DSP's and FPGA's. The Power subsystem derives these voltages from standard VME supply voltages, provides current limiting and soft startup, and enforces any power sequencing rules.

**Clock Generation.** Several different clocks are distributed across the ROD. The Clock subsystem derives these clocks from on-board oscillators or front-panel or backplane clocks. The frequency of most clocks can be set by software.

**VME Interface.** The VME interface allows a VME CPU (i.e., the ROD Crate Controller, or RCC) to control and monitor the ROD. The ROD is a VME slave. The following appear in the memory space mapped to a ROD: a dual-port RAM, a read-only FIFO, and a small set of hardware registers. The VME interface supports the most common bus cycle types, including 64-bit block transfers.

**Host.** The Host subsystem consists primarily of a DSP Module (see below). The Host orchestrates most activities on the ROD. The Host acts as a slave to the ROD Crate Controller, executing commands passed to it via the VME interface.

**Decoders.** Each Decoder consists of a DSP Module (see below). The Decoder is the main data processing and storage element on the ROD. It receives raw event data (via the Interconnect subsystem), buffers it until it can be processed, processes it, and stores the result until it is requested by the Data Exchange subsystem. The Decoders act as slaves to the Host.

**Decoder Control.** The Decoder Control subsystem gives the Host access to the memory space of the Decoders. This access is used to download executable code into the Decoders, transfer per-event information to and from the Decoders, and read out bulk monitoring data such as histograms. For example, the Host passes event ID information for each event to the Decoders and reads back status information for each event. Decoder Control accesses can target any subset of Decoders.

**Data Exchange.** The Data Exchange is a general-purpose unidirectional data transfer mechanism. It can build events by combining data from the Host and Decoders. It can capture a copy of an event for readout by VME (via the Host). The Data Exchange outputs data to the P0 backplane connector. Typically the transition module contains an S-Link that forwards the data to the Readout Buffer (ROB).

**Interconnect.** The Interconnect subsystem interfaces other ROD subsystems to the transition module (i.e., back-of-crate card). It consists of several FPGA's that can be configured to route signals to or from the transition module via the P2, P5, and P6 backplane connectors. The Interconnect subsystem assists ROD self-test. For example, data generated by one half of the ROD can be routed to the other half, or one full ROD can be configured to output data (via a ribbon cable) to a ROD under test.

## Decoder (= DSP Module)

This is the second page of the ROD architecture block diagram. It shows details of the DSP Module that is used for both Decoders and Host. The module consists of a Xilinx Spartan II FPGA, a Texas Instruments C6000 series DSP, a synchronous DRAM chip, and buffers. The FPGA interfaces the DSP's expansion bus to the outside world. It contains logic and buffering needed to convert data to/from a form that can be conveniently DMA'd to/from DSP internal memory. The module size is approximately 2.6 x 2.6 inch or 66 x 66 mm. Its cost is approximately \$300. The module is designed to be replaceable. Connection is via a single 10 pin x 30 pin surface-mount connector.

## CSC Off-Detector Electronics Crates (Front View of Rack)

A front view of the CSC rack is shown. Each Sparsifier crate contains sixteen Sparsifier modules. The ROD crate contains eight ROD's, blank face plates are installed in every other slot for optimal cooling and cable routing. MXI is an off-the-shelf VMEbus extender manufactured by National Instruments. It will make the VMEbus's of all three crates appear as a single VMEbus to the RCC. The TIM (Timing Interface Module) is an ATLAS standard module that delivers clock and trigger signals to each slot in the crate.

## Example Transition Modules (Side View of Rack)

Transition module details are not solidified at this time. One option is shown in this side view of the CSC rack. Each ROD is fed data from four Sparsifiers—only two are shown. The Sparsifier transition module is 400 mm deep, the ROD transition module is 160 mm deep. The 400 mm deep transition module may be necessary because of both area and power constraints. 400 mm transition modules are allowed to dissipate 70 W while 160 mm deep transition modules may only dissipate 28 W. All three crates have identical custom backplanes in the J5/J6 area.

ATLAS standard crates are described at:

[http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/documents/crate\\_od.pdf](http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/documents/crate_od.pdf)

## ROD/Sparsifier Layout

A fairly detailed floorplan of the ROD is shown.

The remaining slides are self-explanatory.