

CSC Electronics Requirements

DOCUMENT IN PRINT
**** WILL BE UPDATED SHORTLY ****

CSC Electronics Interfaces to the Trigger/DAQ System

The CSC Electronics has three interfaces to the ATLAS Trigger/DAQ System: (1) to the Timing, Trigger, and Control (TTC) System, (2) to Readout Buffers (ROBs), and (3) to a local area network. The TTC System provides the CSC Electronics with trigger, timing, and control signals that are time critical. The CSC Electronics outputs its event data to the Readout Buffers. The local area network provides a mechanism for initialization and control of the CSC Electronics and a mechanism for the CSC Electronics to provide monitoring data (for data flow and performance monitoring) to the Trigger/DAQ System.

This document states the requirements placed upon the CSC Electronics by the interfaces to the Trigger/DAQ System.

Interface to TTC System

1. Input from TTC

The CSC off-detector electronics must receive timing, trigger, and control signals from the ATLAS TTC System. It is anticipated that this interface will be provided by a Timing Interface Module (TIM) being designed at University College London by the SCT off-detector electronics group. The TIM will receive TTC signals from a fiberoptic link via a standard TTCrx chip, and it will output relevant TTC signals to a custom crate backplane.

The following TTC-related signals are required for use by the CSC off-detector electronics:

- 40MHz bunch crossing clock: *BC*
- Bunch crossing (BC) counter reset: *BCR*
- Level 1 accept: *L1A*
- Event (L1A) counter reset: *ECR*
- Bunch crossing count identifier: *ROD_BCID*
- Event count identifier: *ROD_LIID*

2. ROD Busy output

The CSC Readout Driver must transmit its ROD_Busy signal via the backplane of the crate to the Timing Interface Module (TIM). The TIM contains the necessary Busy logic to interface to the LVL1 Central Trigger Processor (CTP).

Interface to Readout Buffers

1. Output to Readout Link

The CSC Readout Driver must be capable of outputting data to a standard ATLAS Readout Link. The output record format and the electrical and mechanical interface must

conform to specifications of the ATLAS Trigger/DAQ group. The prototype implementation of the Readout Link is an S-link.

2. Flow control on Readout Link

The CSC Readout Driver must implement the flow control mechanism defined by the Readout Link. This mechanism is defined in the document *Preliminary Interface Specification: ROD99 to Readout Link*.

3. Readout rate

The CSC Readout Driver must be capable of transmitting individual output records. It must be capable of transmitting output records at a rate of 100kHz.

4. Channel ordering

At present, there is no specification on the channel ordering in the output event record from the CSC off-detector electronics.

5. Event ordering

The CSC off-detector electronics must transmit output event (or calibration) records in event order (*i.e.* the order in which they occurred in time).

6. Readout Link test mode

The CSC Readout Driver must provide a diagnostic mode in order to test the Readout Links *in situ*.

Interface to local processing

1. Local area network

The preferred means of controlling the CSC off-detector electronics is via a local area network (presently presumed to be Ethernet) connected to VME-based single board computers (ROD Crate Controllers, or RCCs).

2. VME interface

The preferred means of controlling the modules within the CSC off-detector electronics is via VME, under the control of the ROD Crate Controllers. Consequently, the CSC Readout Driver and Sparsifier Module must implement VME slave interfaces with 32-bit address and data. This interface should incorporate the following VME operations:

- block transfer
- programmed i/o

response to broadcast commands
interrupt generation

3. Configuration and monitoring via VME

The CSC off-detector electronics must be capable of being configured and monitored via VME. Configuration includes setting of status registers and control of operating mode. Monitoring includes read back of contents of status registers and status of current operating mode.

4. Interrupt upon fatal errors

The CSC off-detector electronics must be capable of issuing a VME interrupt when a fatal error condition occurs.

5. Disable or reset via VME

The CSC off-detector electronics must provide the capability to be disabled or reset from VME.