

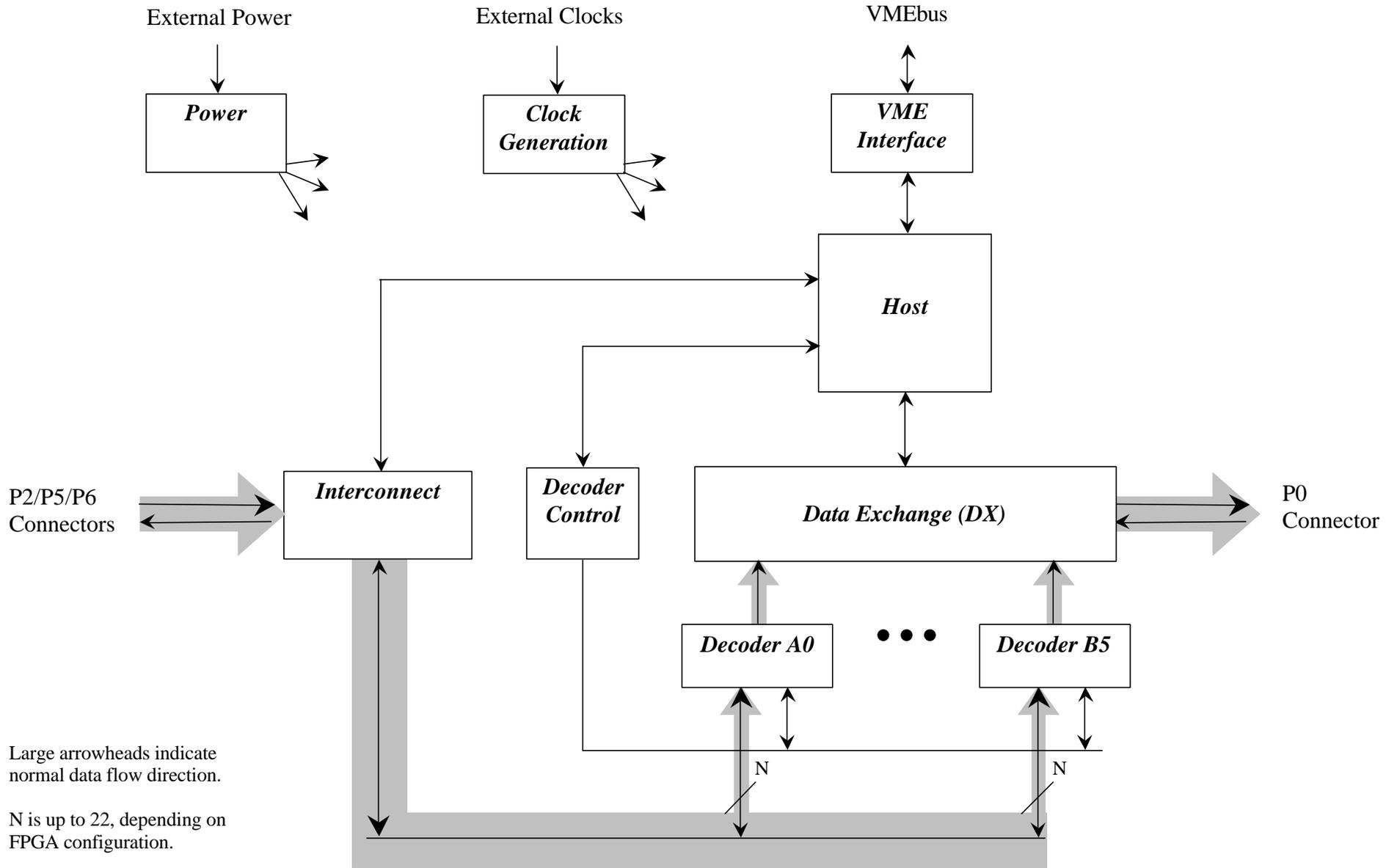
Contents:

IROD Subsystems  
*Decoder* (= DSP Module)  
*Data Exchange (DX)*  
*Host*  
*VME Interface*  
*Decoder Control*  
*Power*  
*Interconnect*  
*Clock Generation*

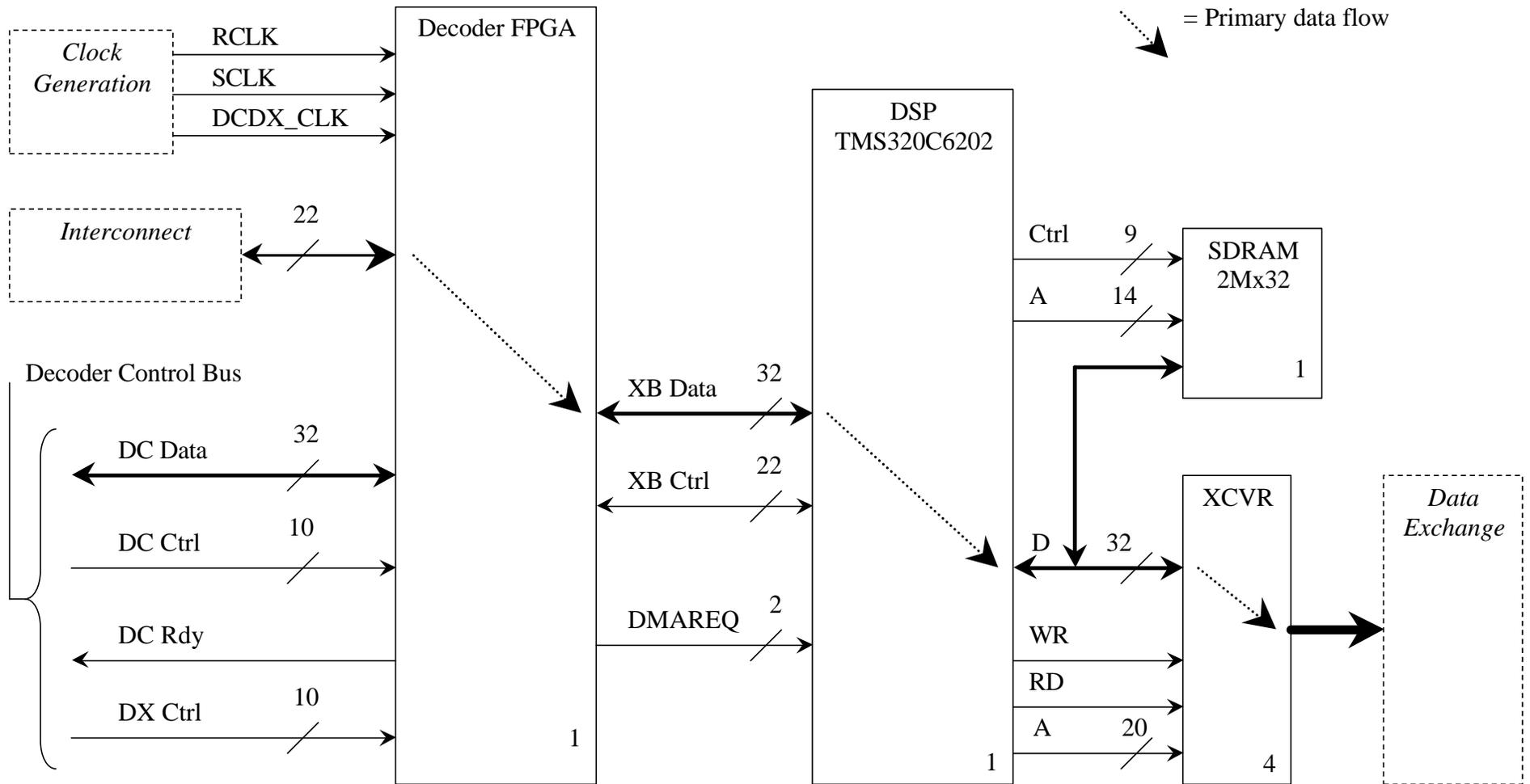
Notes:

Subsystem names are in italics.  
Chip counts appear in the lower right corner of some blocks.  
Many signals are omitted for clarity.

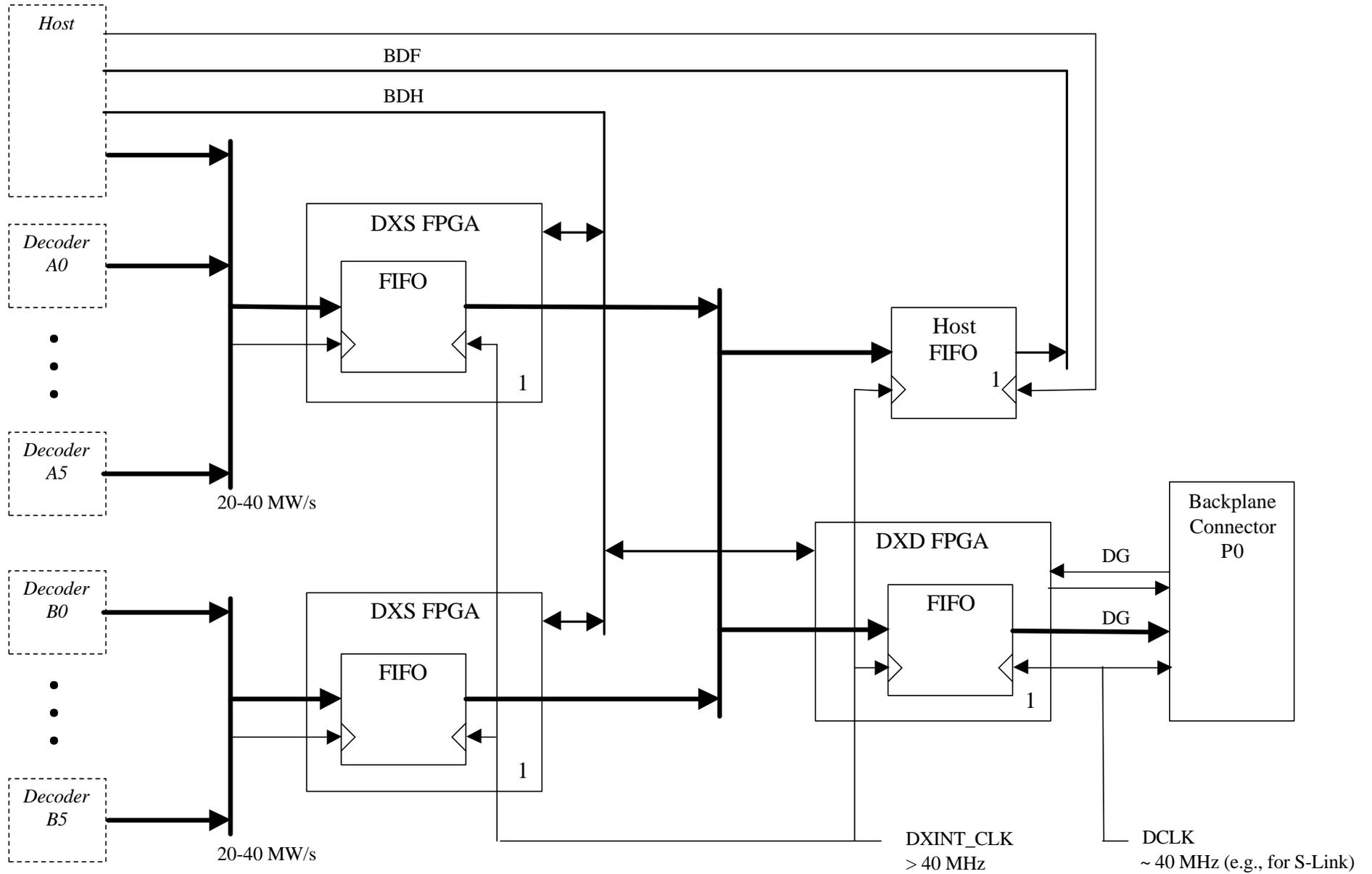
# IROD Subsystems



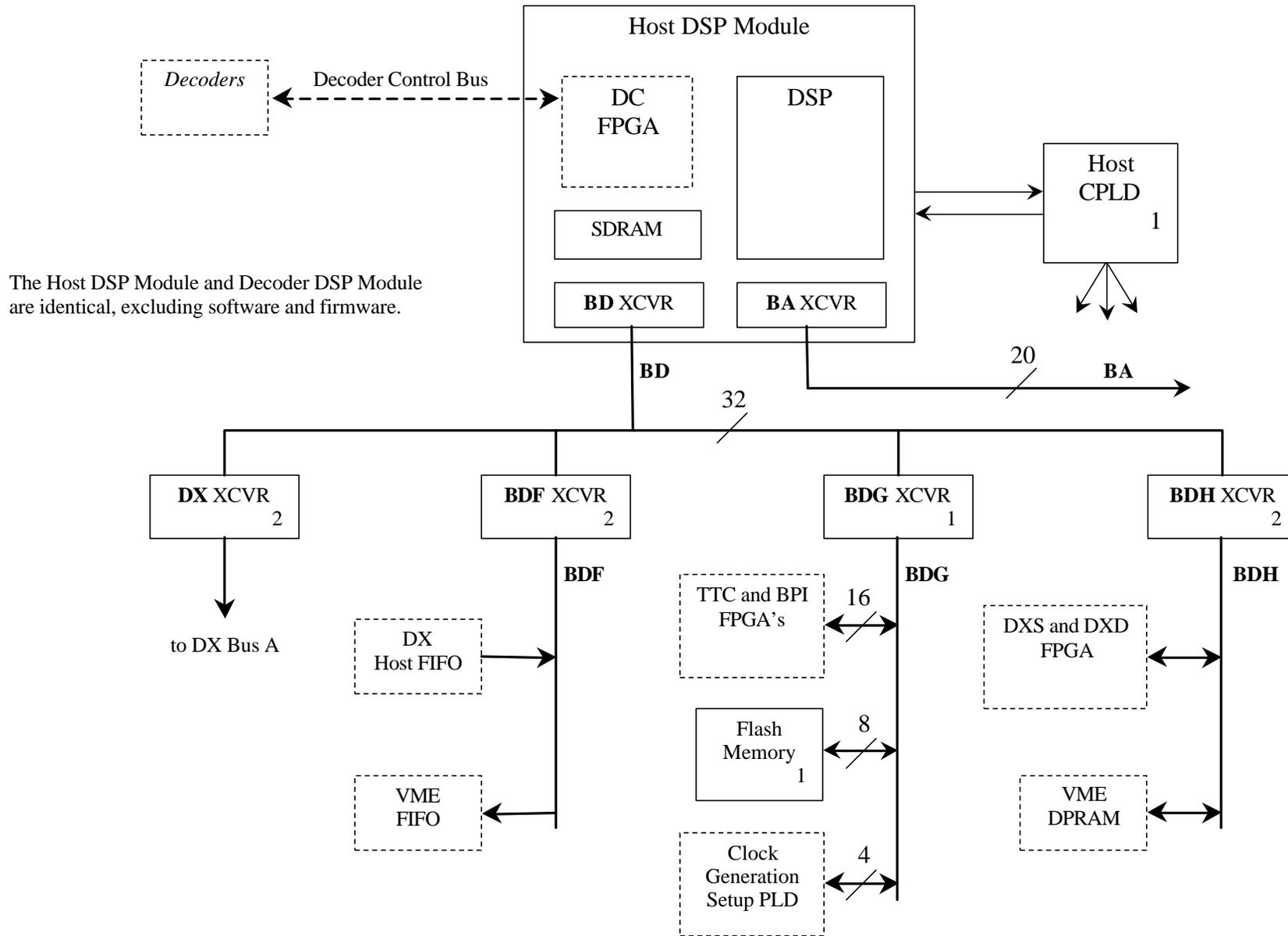
## Decoder (= DSP Module)



# Data Exchange (DX)

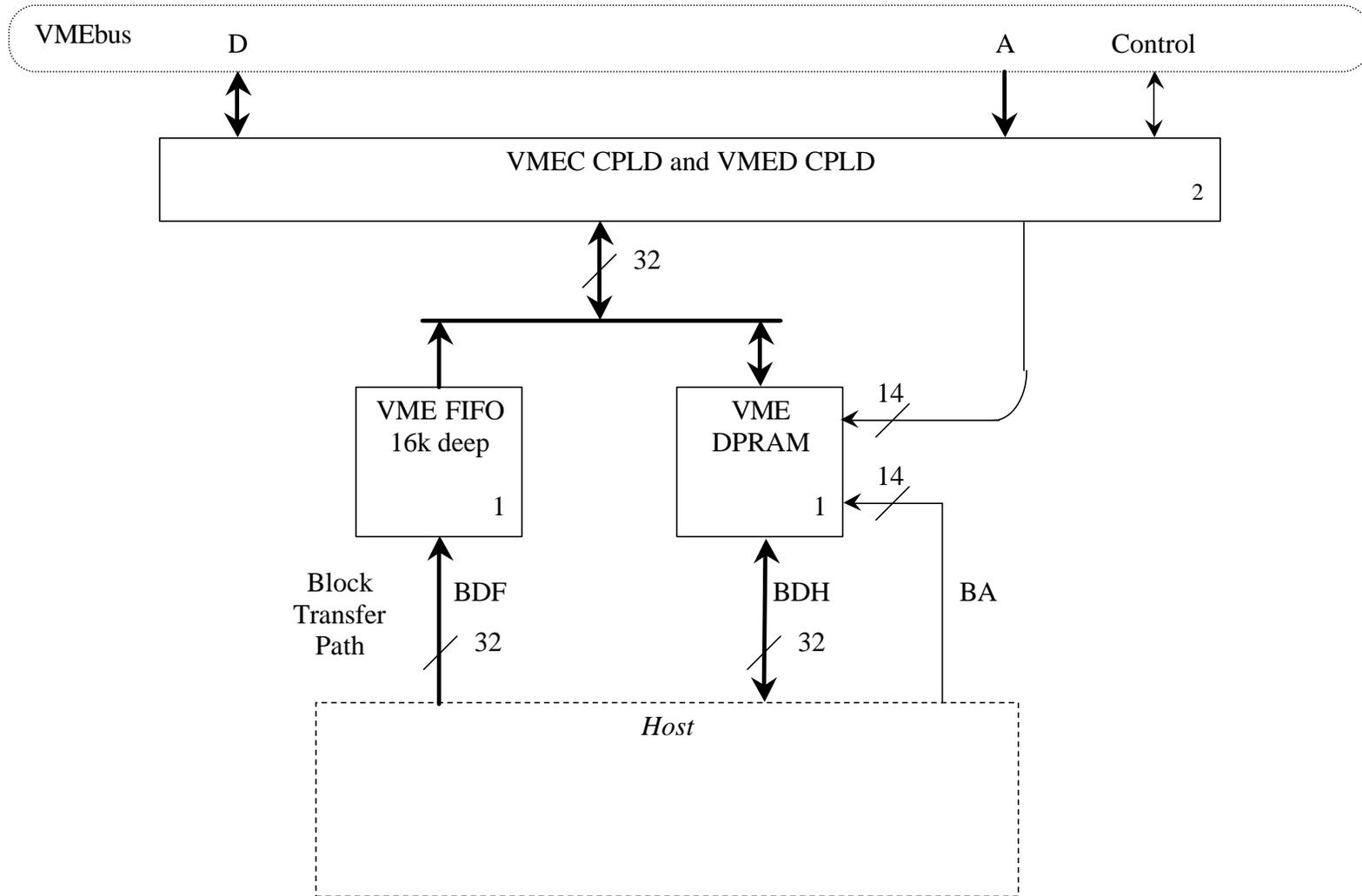


# Host



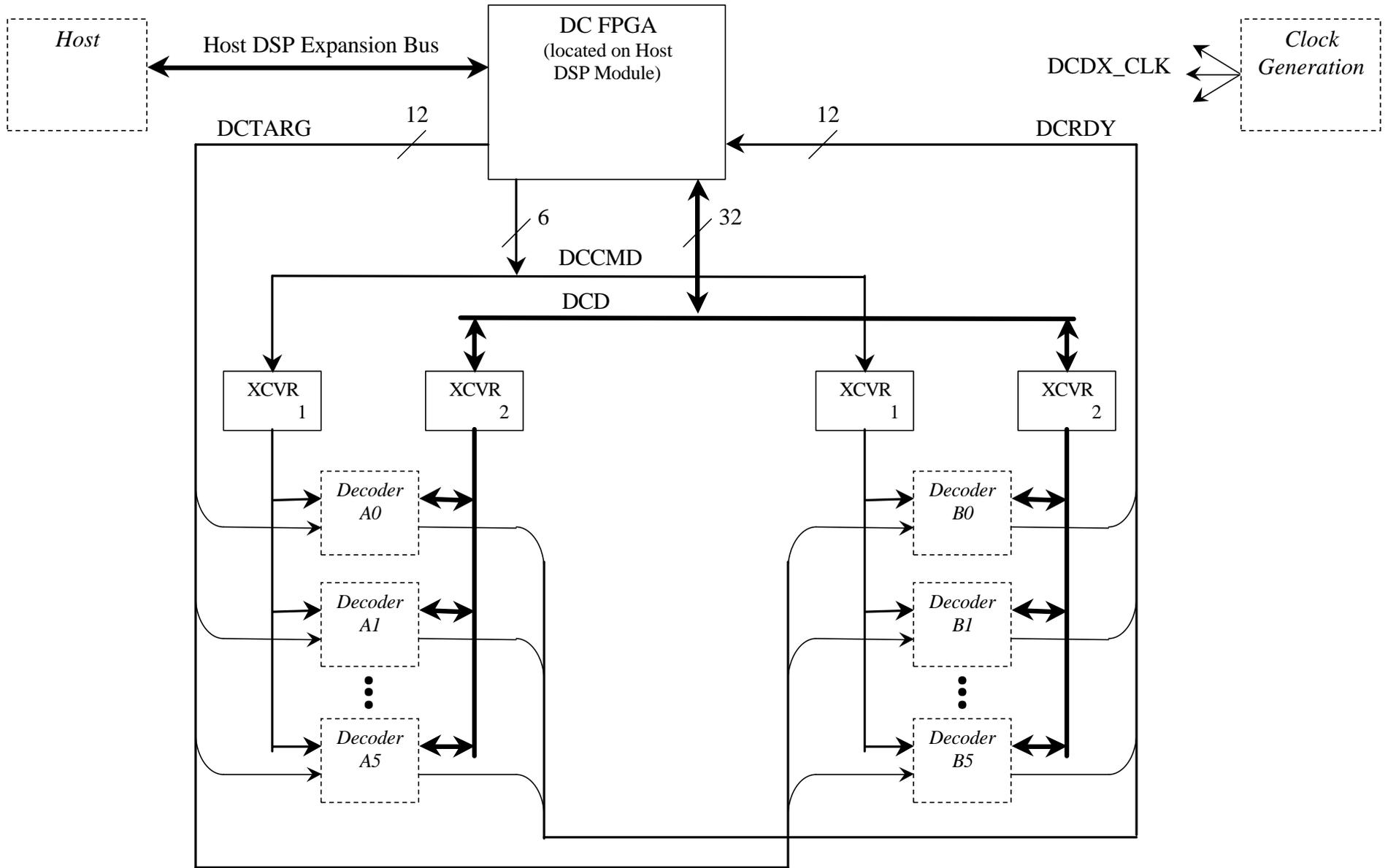
The Host DSP Module and Decoder DSP Module are identical, excluding software and firmware.

# VME Interface

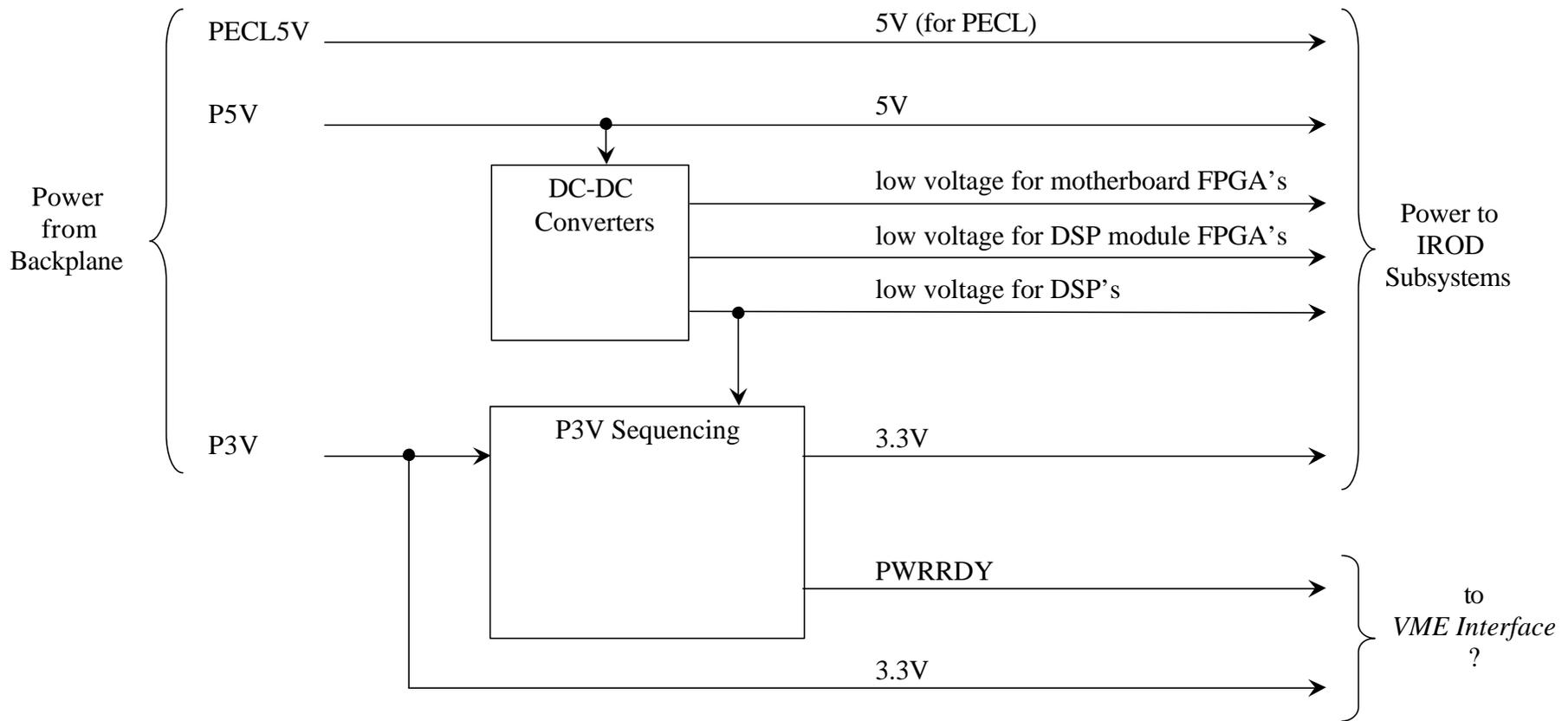


Not Shown:  
 Buffers  
 CS/CSR flash memory  
 Boot flash memory

# Decoder Control (DC)



# Power

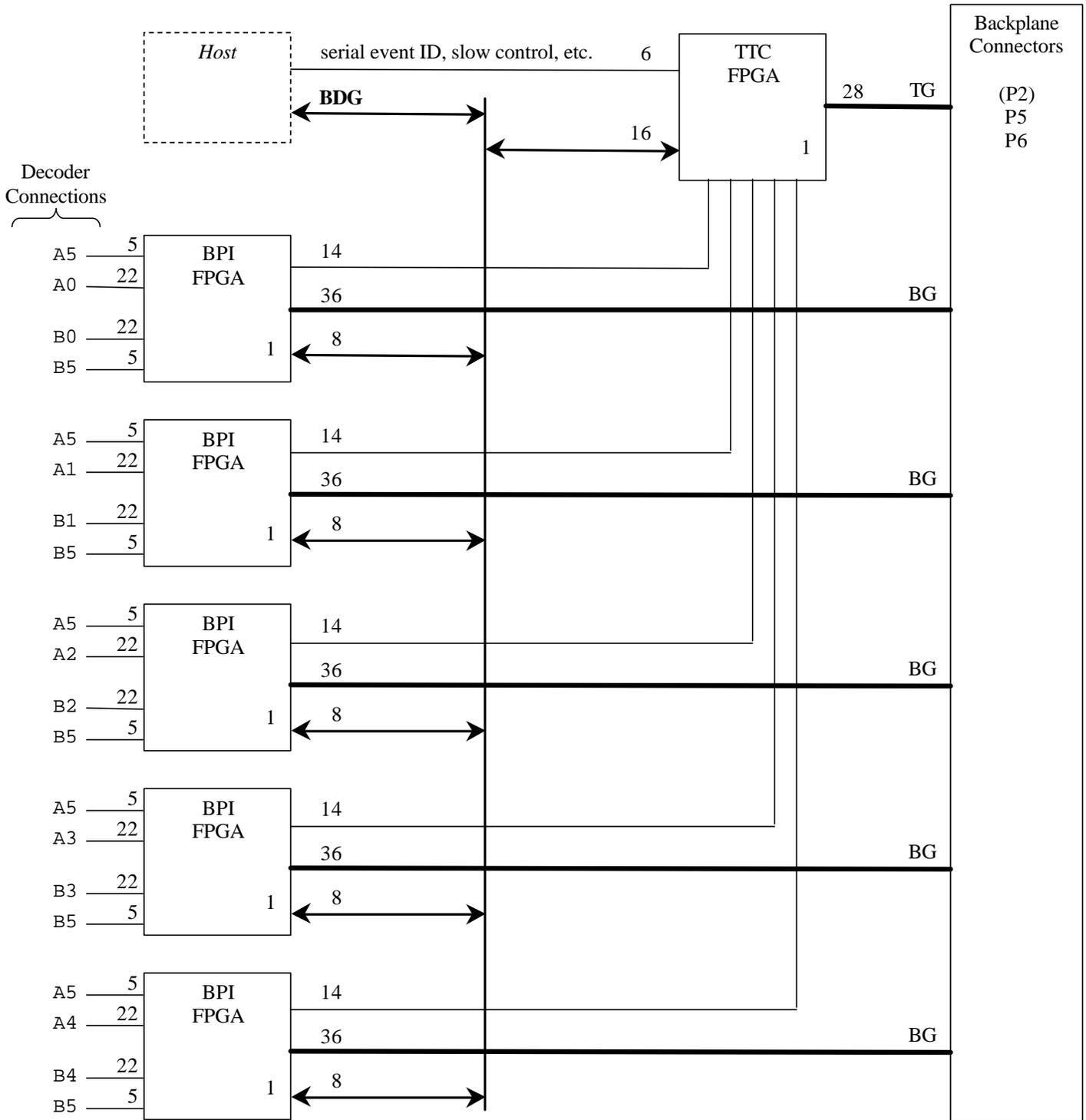


typical FPGA low voltage:  $\leq 2.5V$

typical DSP low voltage:  $\leq 1.8V$

DC-DC converters could use 5V and/or 3.3V for input.

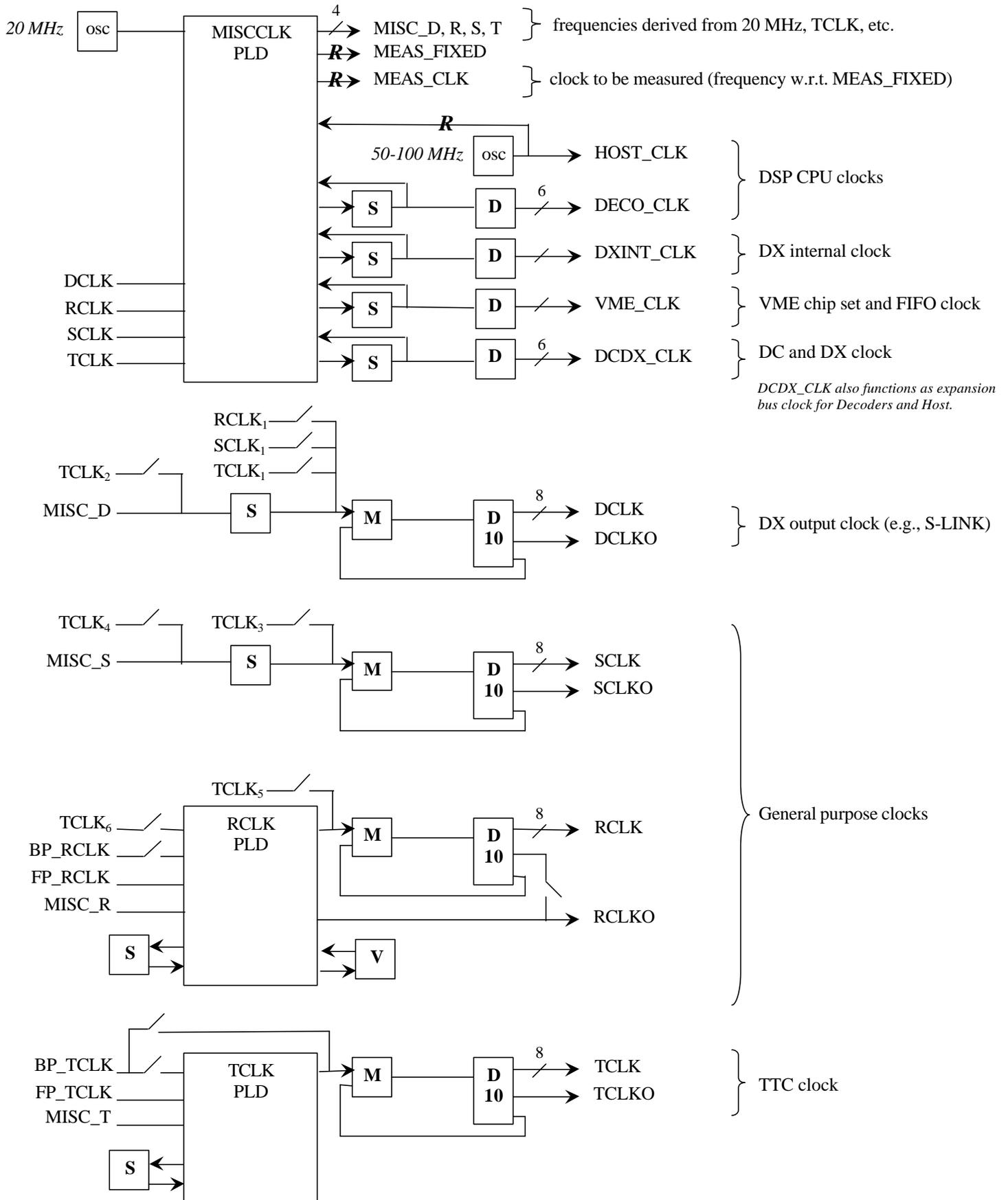
# Interconnect



Total Decoder connections: 270  
 Total backplane connections: 208

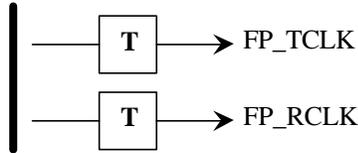
Not shown: each FPGA receives RCLK, SCLK, TCLK, and DCDX\_CLK.

# Clock Generation

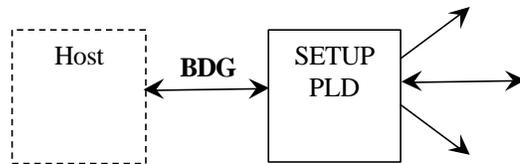


## Clock Generation (Continued)

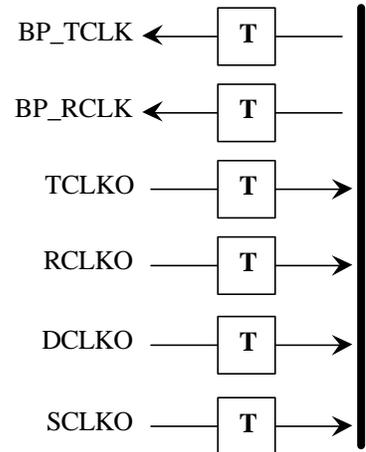
Front Panel



*setup signals to PLD's and other components*



Backplane



**R** = series resistor.

**BP** = backplane, **FP** = front panel.

Setup details are not shown.

**M**'s are zero-delay buffers that can multiply frequency by 1, 2, 4, or 8.

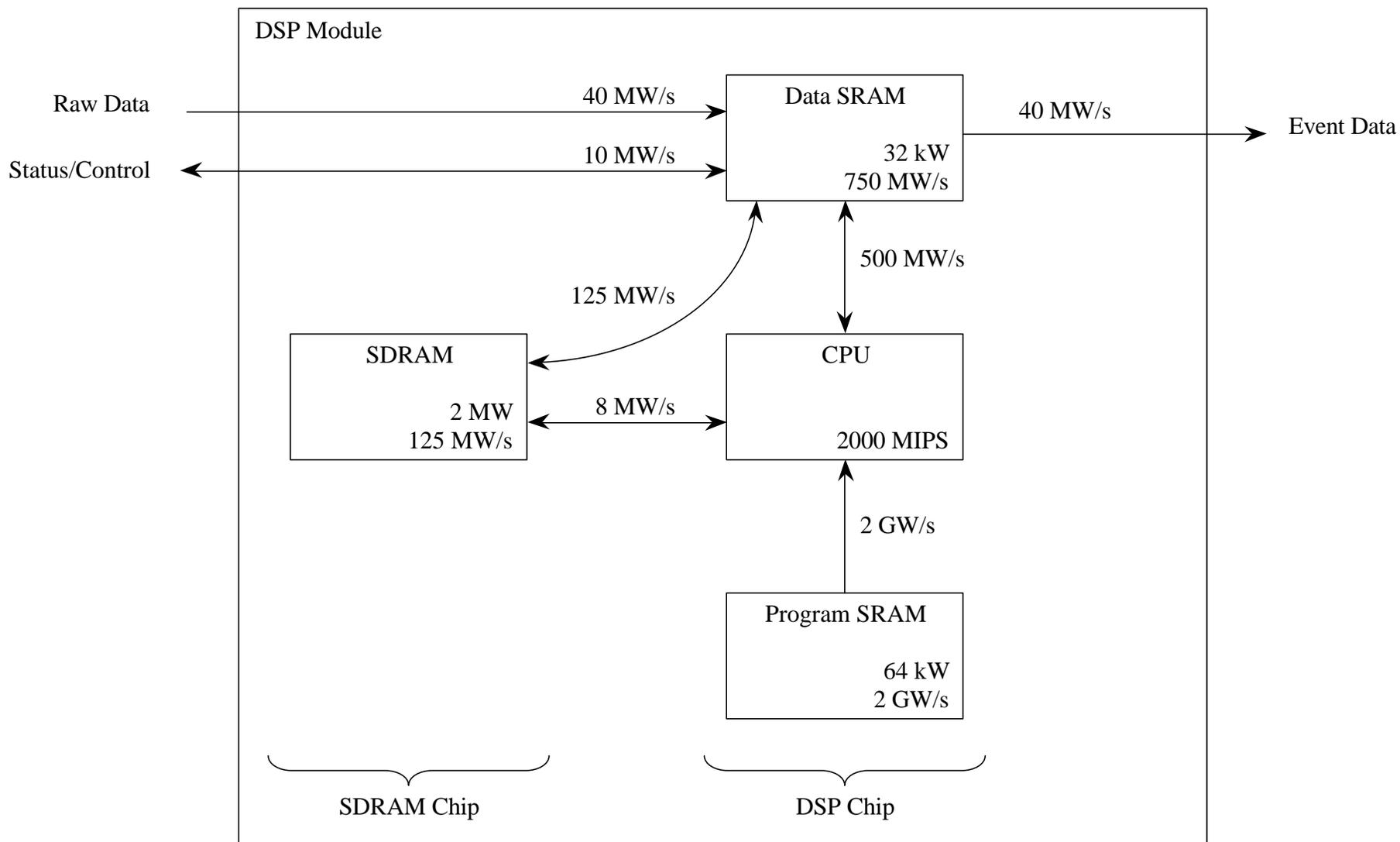
Component summary:

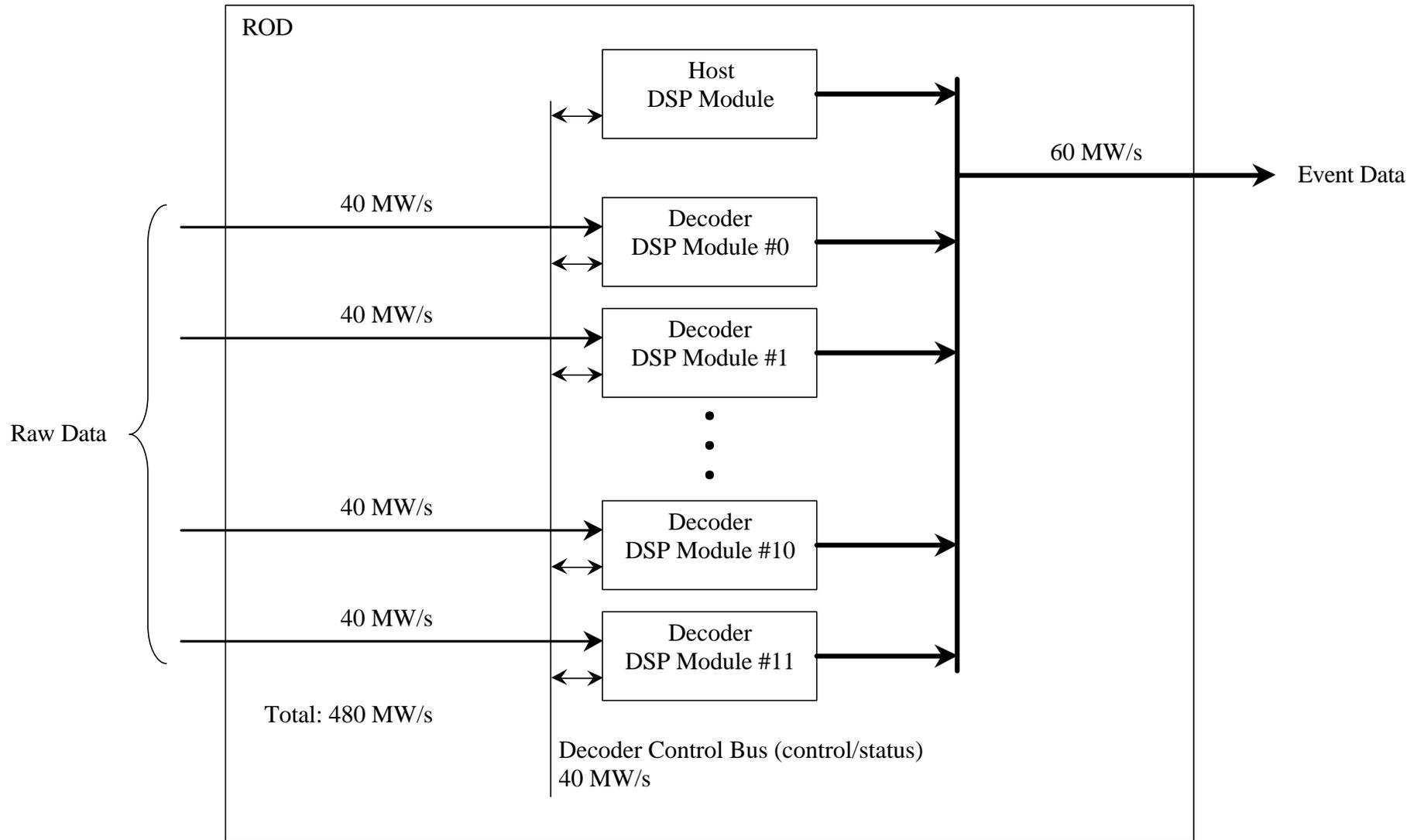
|              | description   | part number  | manu | fmin<br>MHz      | fmax<br>MHz       | skew<br>ps | jitter<br>ps |  | N         | \$each | \$tot        |
|--------------|---------------|--------------|------|------------------|-------------------|------------|--------------|--|-----------|--------|--------------|
| <b>PLD</b>   | CPLD          | XC9572XL     | XC   |                  |                   |            |              |  | 4         | 5      | 20           |
| <b>S</b>     | synthesizer   | ICD2053B     | CY   | in: 1<br>out: .4 | in:25<br>out: 100 |            | no spec      |  | 8         | 4      | 32           |
| <b>D10</b>   | 10-out driver | CDC319       | TI   | 0                | >100              | 250        | no spec      |  | 4         | 2      | 8            |
| <b>D</b>     | 6-out driver  | W40C06A      | CY   | 0                | 100               | 400        | 300          |  | 4         | 2      | 8            |
| <b>M</b>     | multiplier    | W170-01      | CY   | out: 10          | out: 133          |            | 500          |  | 4         | 2      | 8            |
| <b>V</b>     | vernier       | AD9501       | AD   | 0                | 12.5              |            | 53 typ       |  | 1         | 14     | 14           |
| osc          | oscillator    | TBD          | TBD  |                  |                   |            |              |  | 2         | 4      | 8            |
| <b>T</b> / — | translator    | TBD          | TBD  |                  |                   |            |              |  | 8         | 4      | 32           |
|              | FET switch    | 74CBTLV1251G | TI   |                  |                   |            |              |  | 12        | 0.5    | 6            |
|              | <b>total</b>  |              |      |                  |                   |            |              |  | <b>47</b> |        | <b>\$136</b> |

Clock Summary:

| Name        | Typical Use  | typ rate, MHz |
|-------------|--|---------------|
| MISC_D      | fixed frequencies derived from 20 MHz oscillator           | 10            |
| MISC_R      |  | 10            |
| MISC_S      |  | 10            |
| MISC_T      |  | 10            |
| BP_RCLK     | receive clock input from backplane                         | 40-80         |
| FP_RCLK     | receive clock input from front panel                       | 40-80         |
| RCLK, RCLKO | receive clock  | 40-80         |
| SCLK, SCLKO | copy of TTC clock, if needed by Host and/or Decoders       | 40            |
| BP_TCLK     | TTC clock input from backplane                             | 40            |
| FP_TCLK     | TTC clock input from front panel                           | 40            |
| TCLK, TCLKO | TTC clock  | 40            |
| HOST_CLK    | host DSP clock (multiplied by PLL in DSP)                  | 50-100        |
| DECO_CLK    | decoder DSP clock (multiplied by PLL in DSP)               | 50-100        |
| DXINT_CLK   | DX internal clock  | 50-70         |
| DCLK, DCLKO | DX output clock, e.g., S-LINK clock (UCLK)                 | 40            |
| VME_CLK     | clock to VME PLD's   | 50            |
| DCDX_CLK    | DC and DX clock, also functions as DSP expansion bus clock | 30-40         |

# DSP Module Performance (250 MHz TMS320C6202)





# IROD Component Area, Cost and Power Estimate

## Scenarios

| Name                        | Data Links | Links per Decoder | Decoders  | Comps | Comp Cost | Power W | Chip Area sq. mm | % of 9U Area |
|-----------------------------|------------|-------------------|-----------|-------|-----------|---------|------------------|--------------|
| <b>IROD CSC ROD</b>         |            |                   | <b>8</b>  | 125   | \$3,399   | 44      | 44860            | 36%          |
| <b>IROD CSC Sparisifier</b> |            |                   | <b>10</b> | 145   | \$3,928   | 51      | 48828            | 39%          |
| <b>IROD SCT96</b>           | 96         | 8                 | <b>12</b> | 165   | \$4,457   | 58      | 52795            | 42%          |

9U VME Area (340x367, single side): 124780

### Scenario notes:

SCT72 and SCT96 scenarios are provided for comparison with earlier cost estimates.

Comp = Component = chips + passives + connectors (does not include printed circuit boards, assembly, etc.)

### Notes for detailed tables below:

FIFO chips are 16k x 36.

DPRAM chips are 16k x 36.

Subsystem names are in italics.

Chip costs are approximate 2000 single-piece costs. Subtract 10%-20% to get 2000 bulk cost.

DSP chip cost includes TI's university discount.

FPGA power is difficult to estimate. 1W is assumed.

The S-LINK is assumed to be on the back-of-crate card and is therefore not included in the estimate.

This estimate is based on the block diagram:

<http://positron.ps.uci.edu/~pier/csc/IRODBlockDiagram4.pdf>

## Per-DSP-Module Details (= Per-Decoder Details)

| Description             | Part no.          | qty       | cost each | area each | pwr each    | cost total   | pwr total   | area total  |
|-------------------------|-------------------|-----------|-----------|-----------|-------------|--------------|-------------|-------------|
| DSP                     | TMS320C6202GJL250 | 1         | \$144     | 740       | 2.30        | \$144        | 2.30        | 740         |
| FPGA                    | XC2S150-5FG256C   | 1         | \$27      | 289       | 1.00        | \$27         | 1.00        | 289         |
| Transceivers            | SN74LVT16245ADL   | 4         | \$3       | 171       | 0.03        | \$10         | 0.13        | 685         |
| SDRAM 2M x 32           | MT48LC2M32B2-7    | 1         | \$20      | 270       | 0.15        | \$20         | 0.15        | 270         |
| Connector (module)      | TBD               | 1         | \$27      | 0         | 0.00        | \$27         | 0.00        | 0           |
| Connector (motherboard) | TBD               | 1         | \$27      | 0         | 0.00        | \$27         | 0.00        | 0           |
| misc. res/cap/etc.      | several           | 1         | \$10      | 0         | 0.00        | \$10         | 0.00        | 0           |
| <b>Total Per-Module</b> |                   | <b>10</b> |           |           | <b>3.48</b> | <b>\$265</b> | <b>3.58</b> | <b>1984</b> |

## Per-ROD Details

| Description             | Part no.             | qty | cost each | area each | pwr each | cost total | pwr total | area total |
|-------------------------|----------------------|-----|-----------|-----------|----------|------------|-----------|------------|
| <i>Data Exchange</i>    |                      |     |           |           |          |            |           |            |
| Source FPGA's (DXS)     | XC2S150-5PQ208C      | 2   | \$22      | 936       | 1.00     | \$44       | 2.00      | 1873       |
| Destination FPGA (DXD)  | XC2S150-5PQ208C      | 1   | \$22      | 936       | 1.00     | \$22       | 1.00      | 936        |
| Host FIFO               | IDT72V3680L15PF      | 1   | \$89      | 352       | 0.17     | \$89       | 0.17      | 352        |
| <i>Host</i>             |                      |     |           |           |          |            |           |            |
| DSP Module              | N/A                  | 1   | \$265     | 1984      | 3.58     | \$265      | 3.58      | 1984       |
| Host CPLD               | XC9572XL-5TQ100C     | 1   | \$8       | 256       | 0.13     | \$8        | 0.13      | 256        |
| Flash memory            | TBD                  | 1   | \$10      | 270       | 0.03     | \$10       | 0.03      | 270        |
| transceivers            | SN74LVT16245ADL      | 7   | \$3       | 171       | 0.03     | \$18       | 0.23      | 1198       |
| <i>VME interface</i>    |                      |     |           |           |          |            |           |            |
| buffer                  | TBD                  | 6   | \$3       | 171       | 0.03     | \$15       | 0.20      | 1027       |
| VMEC, VMED CPLD's       | XC95288XL-7TQ144C    | 2   | \$24      | 256       | 0.13     | \$48       | 0.26      | 512        |
| Flash CPLD              | XC9572XL-5TQ100C     | 1   | \$8       | 256       | 0.13     | \$8        | 0.13      | 256        |
| Flash memory            | TBD                  | 1   | \$10      | 270       | 0.03     | \$10       | 0.03      | 270        |
| VME FIFO                | IDT72V3680L15PF      | 1   | \$89      | 352       | 0.17     | \$89       | 0.17      | 352        |
| VME DPRAM               | CY7C056V20AC         | 1   | \$86      | 400       | 0.64     | \$86       | 0.64      | 400        |
| <i>Decoder Control</i>  |                      |     |           |           |          |            |           |            |
| DC FPGA                 | (on Host DSP module) | 0   | \$0       | 0         | 0.00     | \$0        | 0.00      | 0          |
| Transceivers            | SN74LVT16245ADL      | 6   | \$3       | 171       | 0.03     | \$15       | 0.20      | 1027       |
| <i>Power</i>            |                      |     |           |           |          |            |           |            |
| DC-to-DC converter      | PT7705C              | 1   | \$51      | 3145      | 0.00     | \$51       | 0.00      | 3145       |
| DC-to-DC converter      | PT6603C              | 2   | \$30      | 1496      | 0.00     | \$60       | 0.00      | 2992       |
| P3V sequencing          | several              | 1   | \$30      | 250       | 0.00     | \$30       | 0.00      | 250        |
| <i>Interconnect</i>     |                      |     |           |           |          |            |           |            |
| TTC FPGA                | XC2S150-5PQ208C      | 1   | \$22      | 936       | 1.00     | \$22       | 1.00      | 936        |
| BPI FPGA                | XC2S150-5PQ208C      | 5   | \$22      | 936       | 1.00     | \$110      | 5.00      | 4682       |
| <i>Clock Generation</i> |                      |     |           |           |          |            |           |            |
| see block diagram       | several              | 1   | \$136     | 1500      | 0.25     | \$136      | 0.25      | 1500       |
| backplane connectors    | TBD                  | 1   | \$100     | 4771      | 0.00     | \$100      | 0.00      | 4771       |
| misc. res/cap/etc.      | several              | 1   | \$50      | 0         | 0.00     | \$50       | 0.00      | 0          |
|                         |                      | 45  |           |           | 9.37     | \$1,283    | 15.03     | 28,990     |

|                                     | <b>6201b</b> | <b>6202</b> | <b>6202b</b> | <b>6203</b> | <b>64xx</b> |
|-------------------------------------|--------------|-------------|--------------|-------------|-------------|
| <b>on-chip program RAM</b>          | .5 Mbit      | 2 Mbit      | 2 Mbit       | 3 Mbit      |             |
| <b>on-chip data RAM</b>             | .5 Mbit      | 1 Mbit      | 1 Mbit       | 4 Mbit      |             |
| <b>L1 program cache</b>             |              |             |              |             | 16 kbyte    |
| <b>L1 data cache</b>                |              |             |              |             | 16 kbyte    |
| <b>L2 cache/direct-map RAM</b>      |              |             |              |             | 1 Mbit      |
| <b>pin-compatible with 6202</b>     | no           | yes         | yes          | yes         |             |
| <b>synchronous expansion bus</b>    | no           | yes         | yes          | yes         |             |
| <b>enhanced throughput DMA</b>      | no           | no          | yes          | yes         |             |
| <b>DMA channels (excluding aux)</b> | 4            | 4           | 4            | 4           | 32          |
| <b>max announced clock rate</b>     | 200 MHz      | 250 MHz     | 250 MHz      | 300 MHz     | 600 MHz     |
| <b>typical power dissipation</b>    | 1.7W         | 2.3W        | (?) 1.5W     | 1.5W        |             |
| <b>available</b>                    | now          | now         | 2000         | samples now | 2001?       |

# Sparsifier Rejection Ratios and Output Rates

|  | case 1   | case 2   | case 3   | case 4   | unit            |
|--|----------|----------|----------|----------|-----------------|
| <b>Cluster width (center channel plus neighbors)</b>                         | <b>5</b> | <b>5</b> | <b>3</b> | <b>3</b> | <b>channel</b>  |
| <b>Sparsifier Acceptance Window, threshold + OOT</b>                         | <b>3</b> | <b>2</b> | <b>3</b> | <b>2</b> | <b>BC</b>       |
| Preamp Pulse Width (time above threshold)                                    | 6        | 6        | 6        | 6        | BC              |
| Beam test occupancy (given acceptance window below)                          | 2%       | 2%       | 2%       | 2%       | cluster/channel |
| Beam test acceptance window (16+Pulse Width -1 )                             | 21       | 21       | 21       | 21       | BC              |
| Sparsifier Acceptance Window, threshold cut only (1+Pulse Width-1)           | 6        | 6        | 6        | 6        | BC              |
| Reciprocal of beam test occupancy  | 50       | 50       | 50       | 50       |                 |
| Sparsifier's zero suppression ratio, threshold cut only                      | 175      | 175      | 175      | 175      |                 |
| Sparsifier's zero suppression ratio, threshold + OOT                         | 350      | 525      | 350      | 525      |                 |
| Sparsifier's zero suppression ratio, threshold cut only, with neighbors >>>> | 35       | 35       | 58       | 58       |                 |
| Sparsifier's zero suppression ratio, threshold + OOT, with neighbors >>>>    | 70       | 105      | 117      | 175      |                 |
| Input bandwidth per chamber (16 bit/sample)                                  | 800.0    | 800.0    | 800.0    | 800.0    | Mbyte/s/chamber |
| Output rate per chamber, threshold cut only >>>>                             | 22.9     | 22.9     | 13.7     | 13.7     | Mbyte/s/chamber |
| Output rate per chamber, threshold + OOT >>>>                                | 11.4     | 7.6      | 6.9      | 4.6      | Mbyte/s/chamber |

## Notes:

Data rates do not include protocol overhead, e.g., header/trailer, a channel number for each cluster, etc.

Beam test occupancy approximates worst case ATLAS occupancy, including the factor of five safety factor.

This spreadsheet models precision channels. Transverse channels have four times higher occupancy, but a cluster width of one channel.

## DSP SCU PERFORMANCE

**Table 1: Clock Cycles Needed for Sparsifier Software**

|   | Clocks Per Channel x Average Channel Count + Clocks of Overhead = Total Clocks |   |     |   |     |             |             |
|---|--|---|-----|---|-----|-------------|-------------|
| <b><u>High Level Code</u></b>               |  |   |     |   |     |             |             |
| Process SCA controller serial data          |  |   |     |   | 100 | = 100       |             |
| Decide whether to discard                   |  |   |     |   | 200 | = 200       |             |
| Function calls overhead                     |  |   |     |   | 100 | = 100       |             |
| Check for errors                            |  |   |     |   | 100 | = 100       |             |
| Misc  |  |   |     |   | 100 | = 100       |             |
| <b>Total</b>                                |  |   |     |   |     | <b>600</b>  |             |
| <br><b><u>Phase 1 Code</u></b>              |  |   |     |   |     |             |             |
| Apply simple threshold                      | 1  | x | 192 | + | 25  | = 217       |             |
| Apply complex threshold                     | 1.5  | x | 192 | + | 25  | = 313       |             |
| Misc  |  |   |     |   | 100 | = 100       |             |
| <b>Total, simple threshold</b>              |  |   |     |   |     | <b>317</b>  |             |
| <b>Total, complex threshold</b>             |  |   |     |   |     | <b>413</b>  |             |
| <br><b><u>Phase 2 Code</u></b>              |  |   |     |   |     |             |             |
| Apply out-of-time test                      | 10   | x | 21  | + | 25  | = 235       |             |
| Mark neighbors                              |  |   |     |   | 50  | = 50        |             |
| Misc  |  |   |     |   | 100 | = 100       |             |
| <b>Total</b>                                |  |   |     |   |     | <b>385</b>  |             |
| <br><b><u>Output Code</u></b>               |  |   |     |   |     |             |             |
| Extract and format to output                | 10   | x | 9   | + | 50  | = 140       |             |
| Misc  |  |   |     |   | 100 | = 100       |             |
| <b>Total</b>                                |  |   |     |   |     | <b>240</b>  |             |
| <br><b>Grand Total, simple threshold</b>    |  |   |     |   |     |             | <b>1542</b> |
| <b>Grand Total, complex threshold</b>       |  |   |     |   |     |             | <b>1638</b> |
| <br><b>Headroom at 100kHz trigger rate:</b> |  |   |     |   |     |             |             |
| <b>Simple threshold, 250MHz DSP</b>         |  |   |     |   |     | <b>958</b>  |             |
| <b>Complex threshold, 250MHz DSP</b>        |  |   |     |   |     | <b>862</b>  |             |
| <br><b>Simple threshold, 300MHz DSP</b>     |  |   |     |   |     | <b>1458</b> |             |
| <b>Complex threshold, 300MHz DSP</b>        |  |   |     |   |     | <b>1362</b> |             |
| <br><b>Simple threshold, 600MHz DSP</b>     |  |   |     |   |     | <b>4458</b> |             |
| <b>Complex threshold, 600MHz DSP</b>        |  |   |     |   |     | <b>4362</b> |             |

# 1 Sparsifier Algorithm

The goal of the present studies at UCI is to demonstrate that data volume can be reduced by simple algorithms implemented in the Sparsifier. Data must be sparsified both in space, suppressing channels that have no signals above threshold, and in time, suppressing signals that are not coincident with the trigger.

Data from the CSCs consist of digitized pulse heights of groups of adjacent strips which exceed a threshold cut. These clusters, typically five strips wide, are used by the off-line analysis to reconstruct the positions of incident tracks. Signals from strips between the clusters are digitized as well, but suppressed by the Sparsifier logic. This data reduction is necessary to transmit the meaningful data within the available bandwidth. Even at an average flux of  $1500 \text{ Hz/cm}^2$ , five times higher than expected, the probability for a hit cluster per beam crossing in one layer is only  $3/8$ .

In addition to suppressing channels without hits, the Sparsifier also suppresses signals which are not in time with the trigger. Rejection of these wrong-time pulses is essential for limiting the bandwidth of the data stream.

The sparsification algorithm operates on the four consecutive time samples of each channel. These samples are spaced 50 ns apart and called  $A$ ,  $B$ ,  $C$  and  $D$ . The peak of an in-time signal of average drift time lies between samples  $A$  and  $C$ . Triggers can occur in any beam crossing (25 ns spacing). If the trigger occurs in phase with the 50 ns sampling clock, then the sampling is called “even”. Otherwise, it occurs between two sampling periods and is called “odd”. Information about this sampling phase is used by the Sparsifier to correct for the resulting 25 ns signal shift. The delay between the trigger and the start of sampling is adjusted until the signal peak occurs at the time of the  $B$  sample for even sampling. For odd sampling, the peak occurs halfway between  $B$  and  $C$ . Figure 1 shows the CSC waveforms for even (top) and odd (bottom) sampling.

In order to reject the channels without hits, a threshold is applied to the biggest sample,  $B$ . This threshold is adjustable to optimize selection efficiency and rejection rates.

For even sampling, wrong-time pulses can be rejected by requiring a rising slope between samples  $A$  and  $B$  and a falling slope between samples  $B$  and  $C$ . This requirement ( $B > A$  and  $B > C$ ) results in an acceptance window that is two beam crossings wide. This width of 50 ns is somewhat larger than

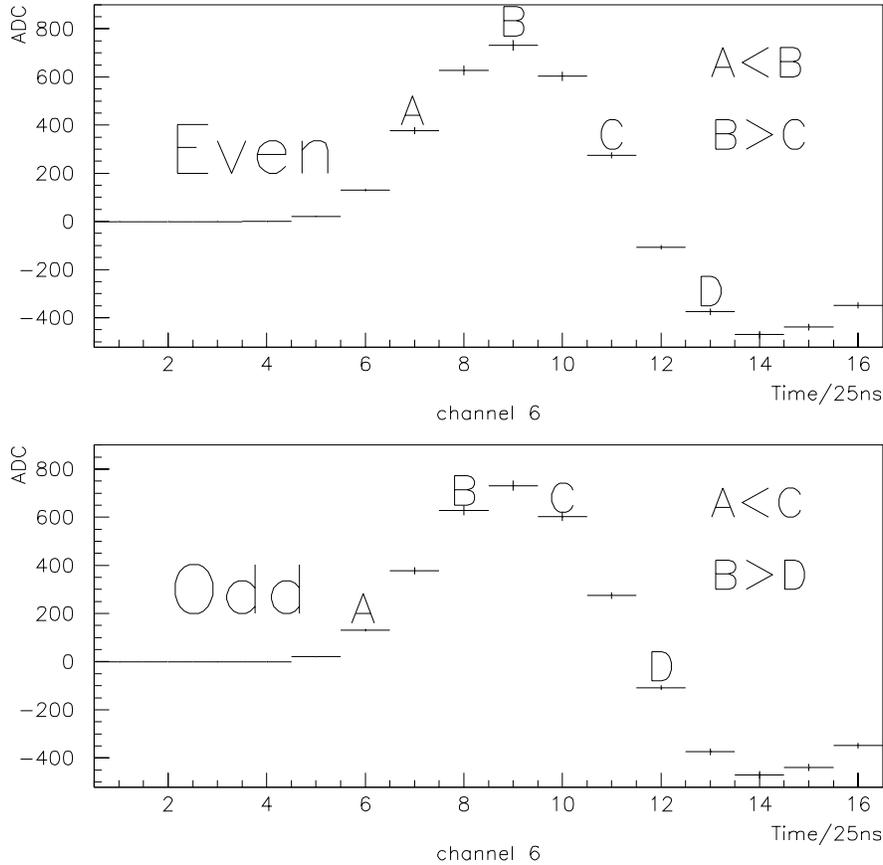


Figure 1: CSC waveforms for even (top) and odd (bottom) sampling of beam test data.

the maximum drift time of 35 ns, ensuring a high selection efficiency over the entire range of drift times.

For odd sampling, the acceptance window has to be shifted by 25 ns to compensate for the shift in the data. The requirement becomes ( $C > A$  and  $B > D$ ) and selects waveforms which peak between the times of the  $B$  and  $C$  samples.

Figure 2 shows the two acceptance windows for beam test data. The top graph is the result of applying the selection requirement for even sampling on data with even sampling. The bottom graph shows the result of the odd sampling selection on the odd-sampled data. Note that the two selection

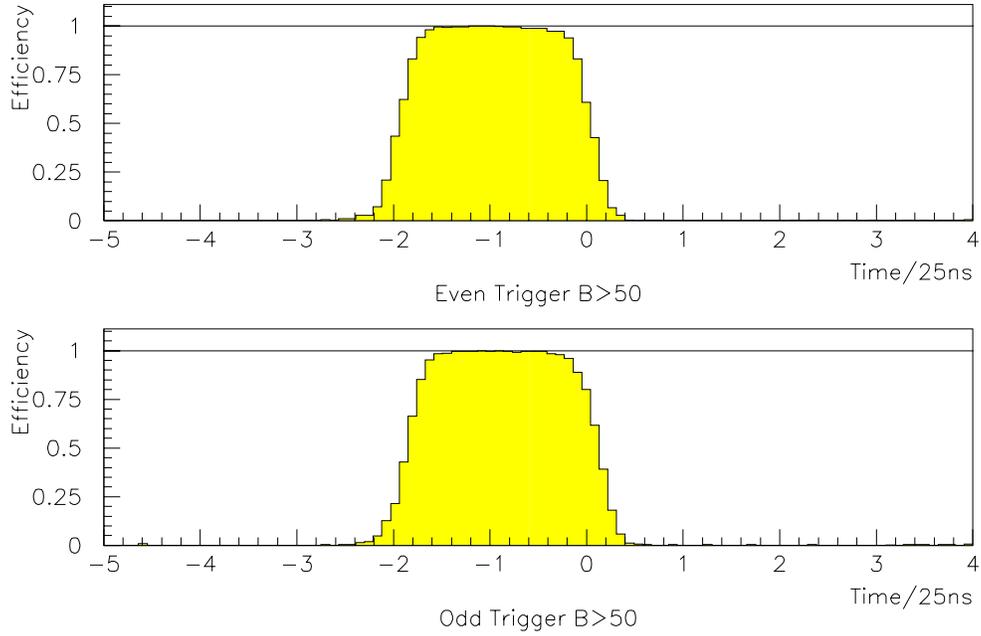


Figure 2: Selection efficiency vs. time for even (top) and odd (bottom) sampling of beam test data.

windows coincide. The selection algorithm was found to be 98.4% efficient within a 35 ns window for a hit rate of 5000 Hz/cm<sup>2</sup>, five times the expected rate. The effectiveness of this algorithm results from the excellent noise performance of the chambers.