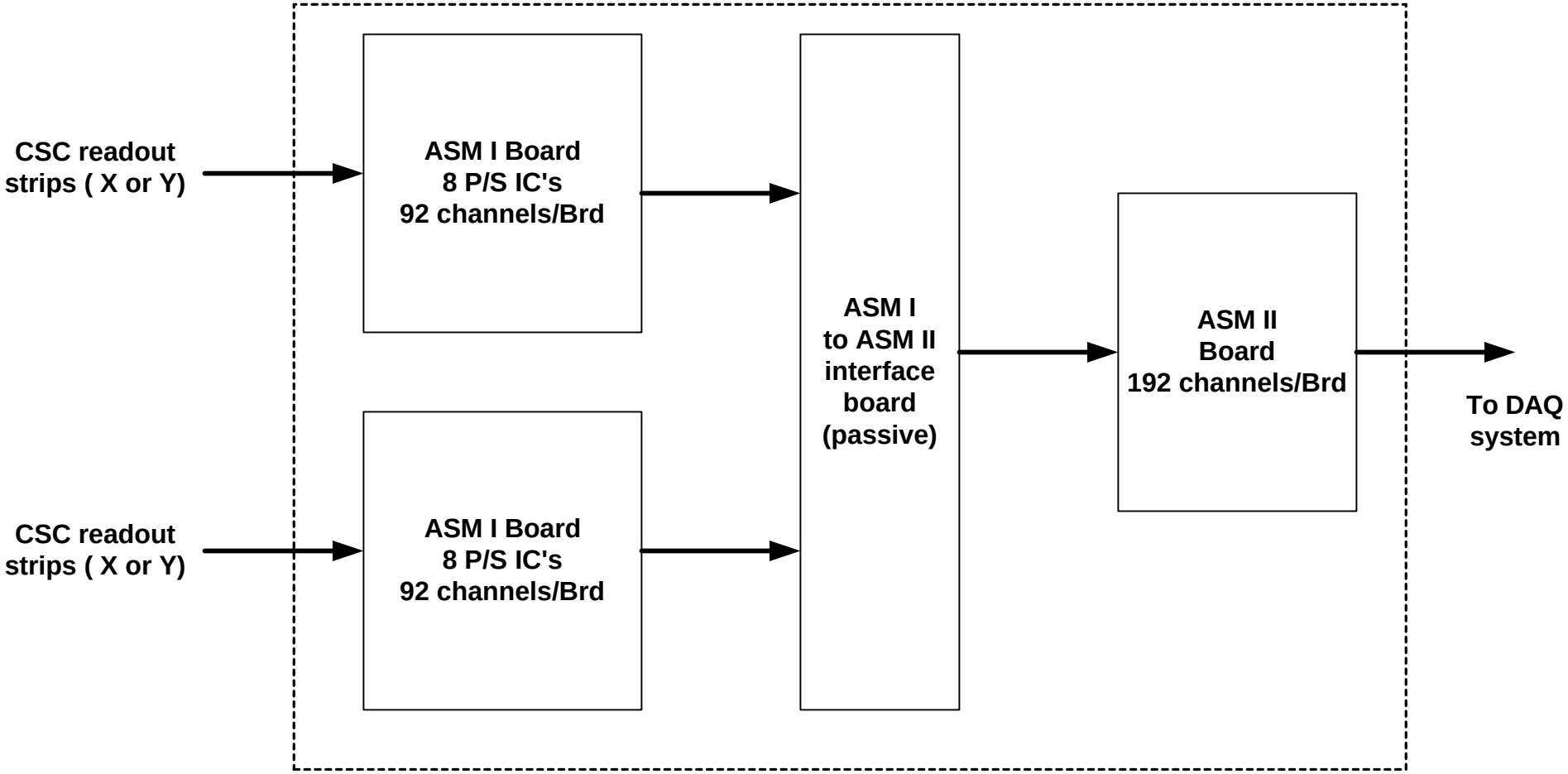
Preliminary Design Review

Amplifier Strorage Module (ASM) Pack

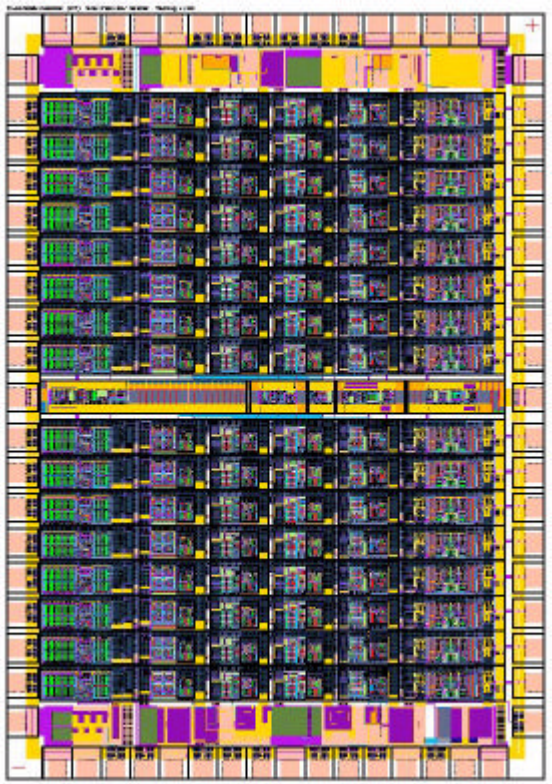


Each ASM Pack consits of 2 - 96 channel ASM I board, an ASM I to ASM II interface board and one 192 channel ASM II board

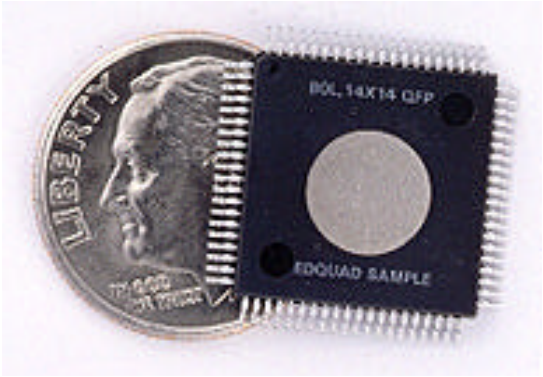
Each CSC chamber requires 5 ASM Packs (2 Left - X strips, 2 Right - X strips and 1 Y strips)

ASM I Board Details

Each ASM I Board consits of 8 CMOS Monolithic integrated circuit performing preamplification and shaping of the detector signals.



Technology	**:**	**0.5 um CMOS**
Channels	**:**	**16**
Die size	**:**	**2.78 mm x 3.96 mm**
Intended Cdet	**:**	**20 to 100 pF**
Noise	**:**	**1150 + 17.6 e-/pF**
Gain	**:**	**3.8 mV/fC**
Max. Linear Q	**:**	**450 fC**
Output Stage	**:**	**Class AB, swings to Power supply - 250mV**
Pulse Peaking Time(5% to 100%)	**:**	**73 ns**
Power Supply	**:**	**+3.3V**
Power Dissipation	**:**	**32.5mW/Channel**



Packaged in 80 Lead, 14 mm x 20 mm EDQUAD QFP

ASM I Board Details

- ASM I Board interfaces to the detector using a card edge connector.

  4 card edge connector / Board

- Analog signals from the ASM I board is shipped to the ASM II board via an intermediate passive board which combines two ASM I boards of 96 channels each and reorders the signals in a manner that is required by the 192 channel ASM II board.

- Board-to-Board stacking connectors are used on the intermediate board to mate ASM I and ASM II together.

- Total Power consumption per ASM I board : 4.2 Watts

- Types of ASM I boards

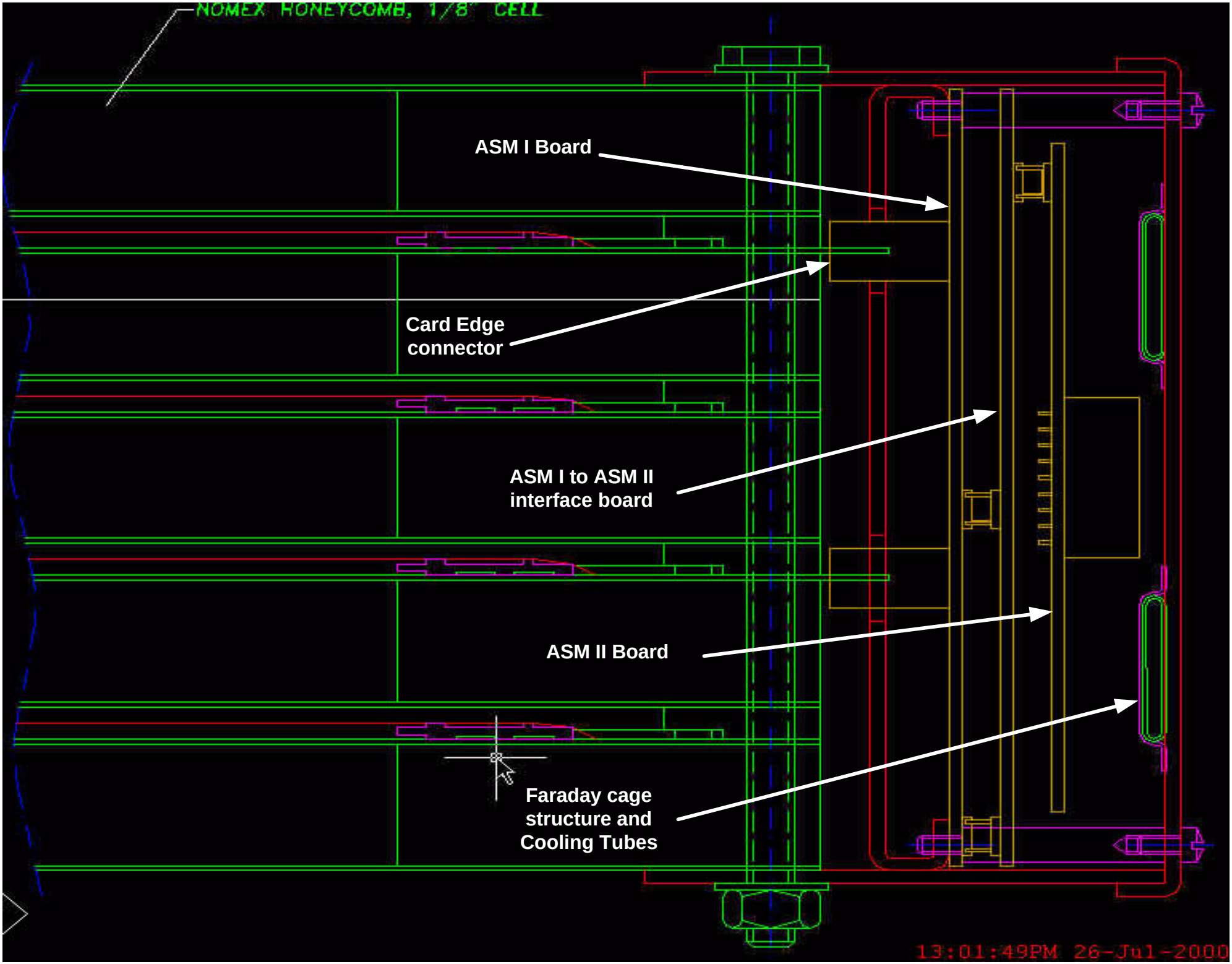
  3 - Left X strip, Right X strip and Y strip.

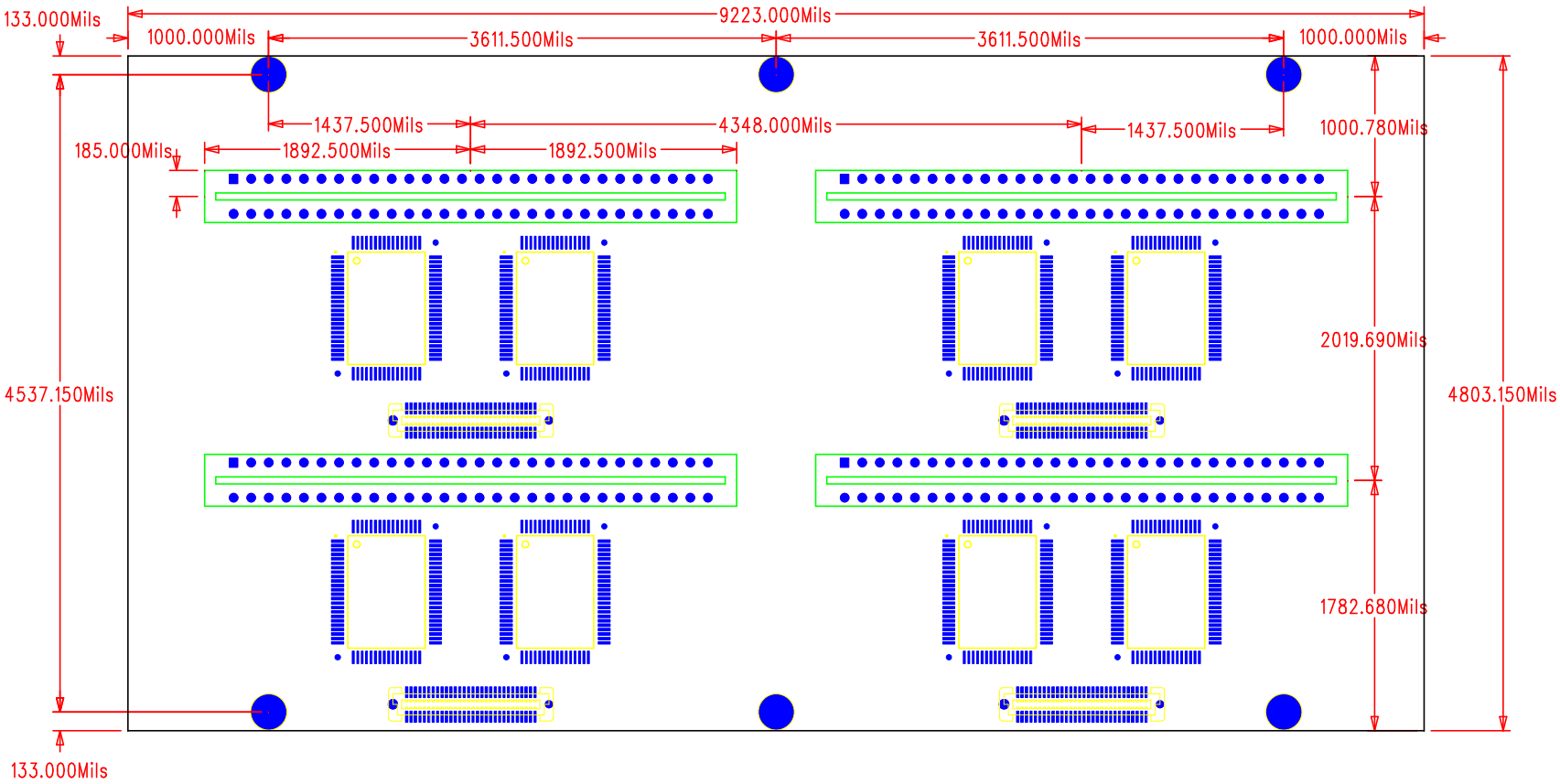
- Two ASM Pack consisting of 2 ASM I's and one ASM II are needed for each side of the chamber namely Left and Right.

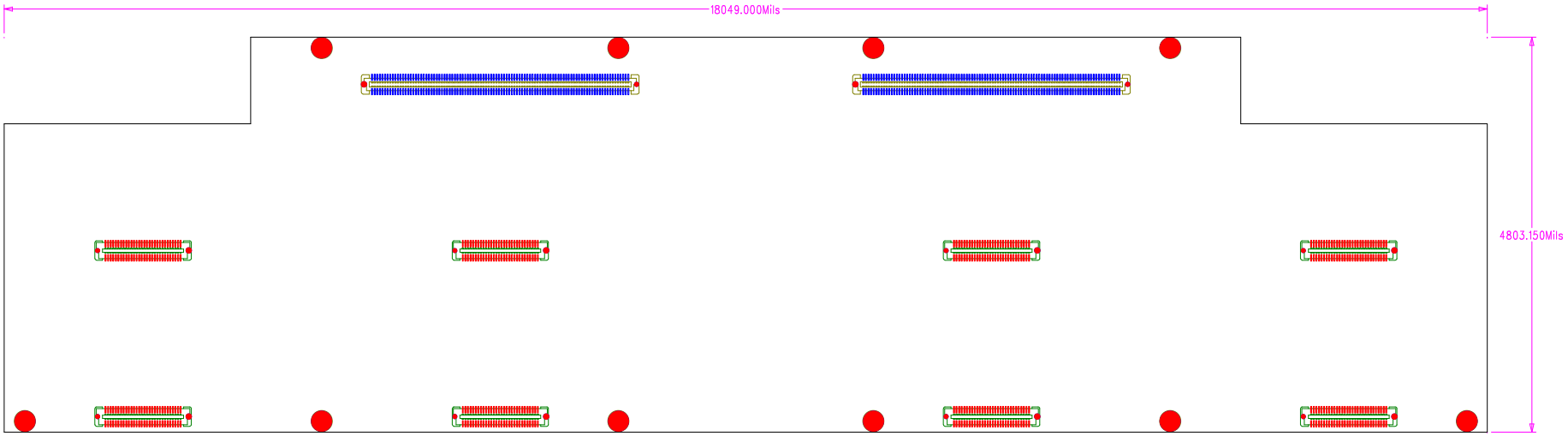
  Plans are to assemble these two ASM packs along with the Faraday Cage and cooling plenum as one single unit facilitating easy testing and installation.

- The Right ASM I board interfaces to Plane 1 and 3 on the Chamber and the Left ASM I board interfaces to Plane 2 and 4.

- ASM I and ASM II GROUND is electrically connected to the Faraday cage using the mounting hardware and the Faraday cage in turn is connected to the top and bottom skins of the chamber which provide the system ground for the electronics.


NOMEX HONEYCOMB, 1/8" CELL
ASM I Board
Card Edge connector
ASM I to ASM II interface board
ASM II Board
Faraday cage structure and Cooling Tubes
13:01:49PM 26-Jul-2000


133.000Mils
9223.000Mils
1000.000Mils
3611.500Mils
3611.500Mils
1000.000Mils
1437.500Mils
4348.000Mils
1437.500Mils
1000.780Mils
185.000Mils
1892.500Mils
1892.500Mils
2019.690Mils
4537.150Mils
4803.150Mils
1782.680Mils
133.000Mils


18049.000Mils
4803.150Mils

Atlas CSC ASMII

Kurt Vetter

Brookhaven National Laboratory

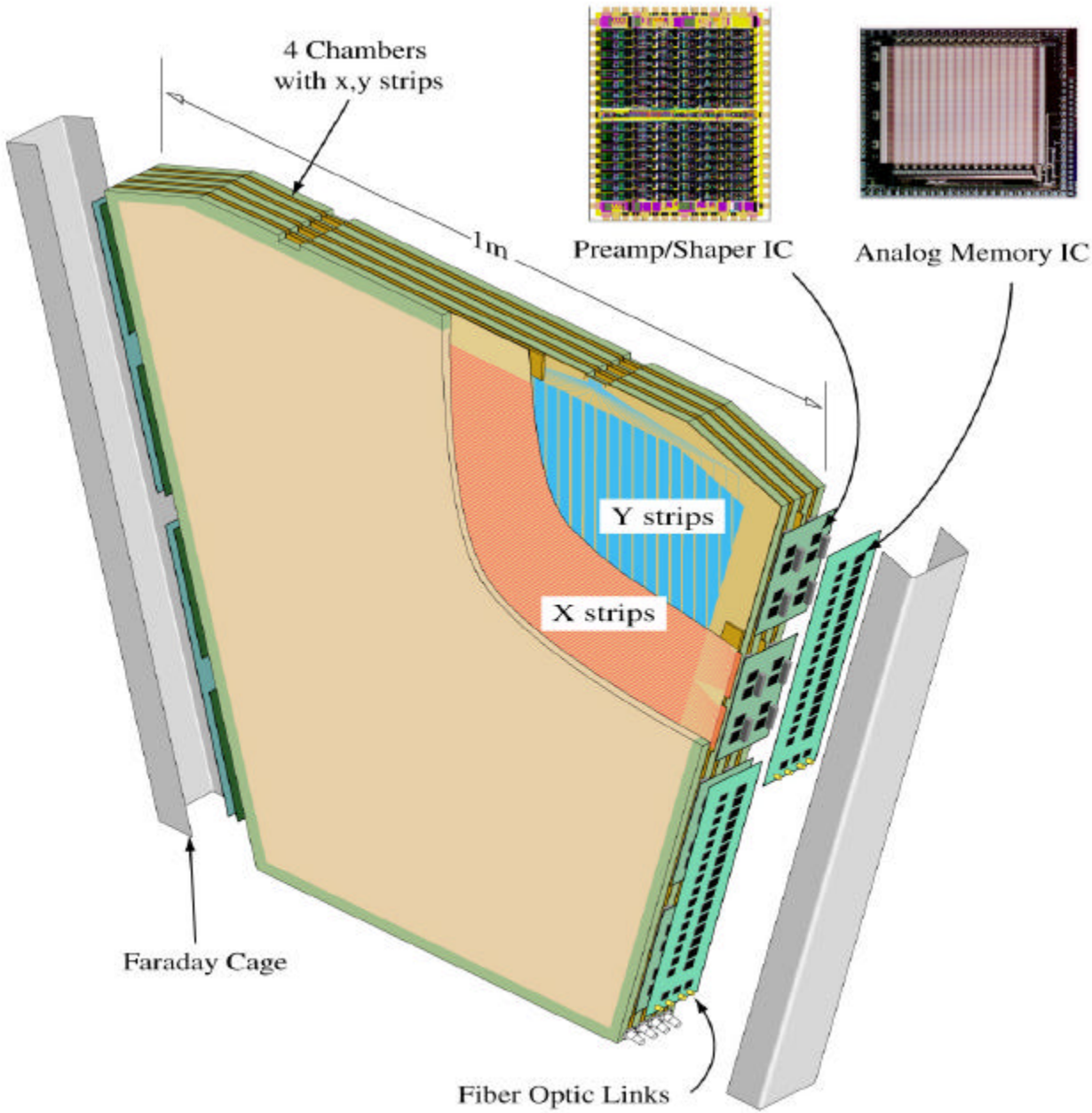
Presented at BNL

August 7, 2000

Topics

1. Introduction and key facts
2. Design Details
3. Optical Links
4. Radiation

ATLAS CSC with Electronics



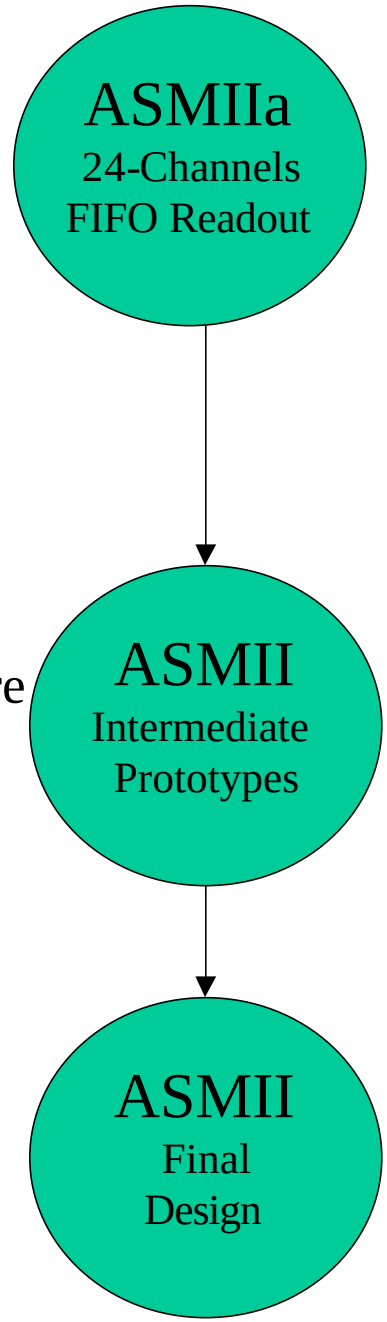
ASMII FACTS

- 5 per chamber
- 4 x-strip (2 per side)
- 1 y-strip
- 320 per system (256 x-strip, 64 y-strip)
- Total Material Cost $629,650
- $2,000 per ASMII
- 192 Channels per ASMII

KEY MILESTONES

- Preliminary Design Review (PDR) – August 2000
- Beam Test – September 2000
- ASMII/Sparsifier Integration – April 2002
- ASMII Final Design Review (FDR) – March 2003
- Production Readiness Review (PRR) – July 2003
- ASMII production begins – August 2003
- ASMII fabrication complete – February 2004
- ASMII installation – April 2004

ASMII Design Evolution



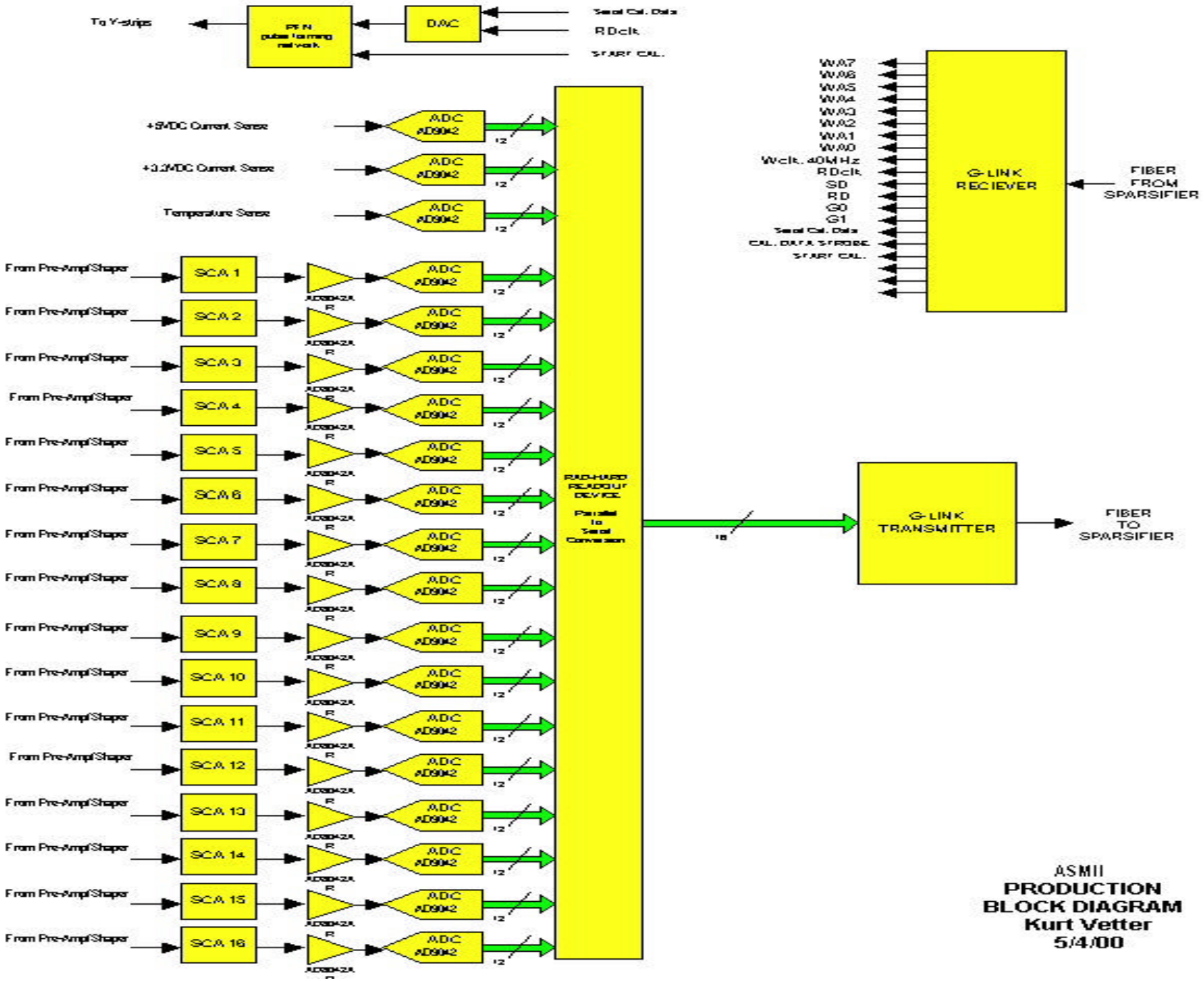
Design Objectives

- Develop SCA Controller
- Test SCA (muon mode)
- Preamp/SCA interface
- Remote SCA control
- Characterize ADC
- Evaluate Noise
- Beam Test Electronics

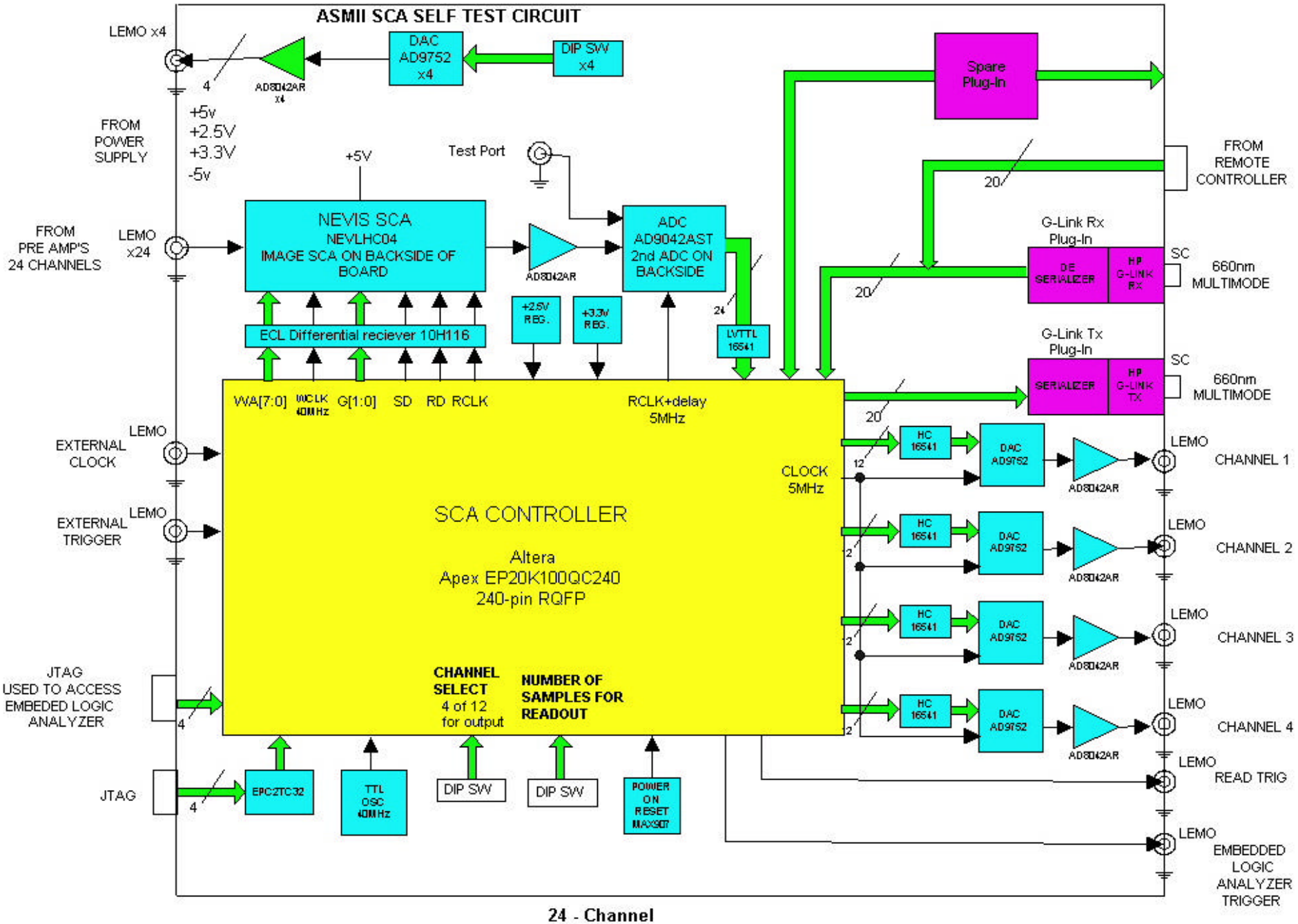
Design Objectives

- 192 Channels
- Develop Readout Architecture
- Develop Optical Link's
- Characterize Noise
- Calibration circuitry

ASMII Block Diagram

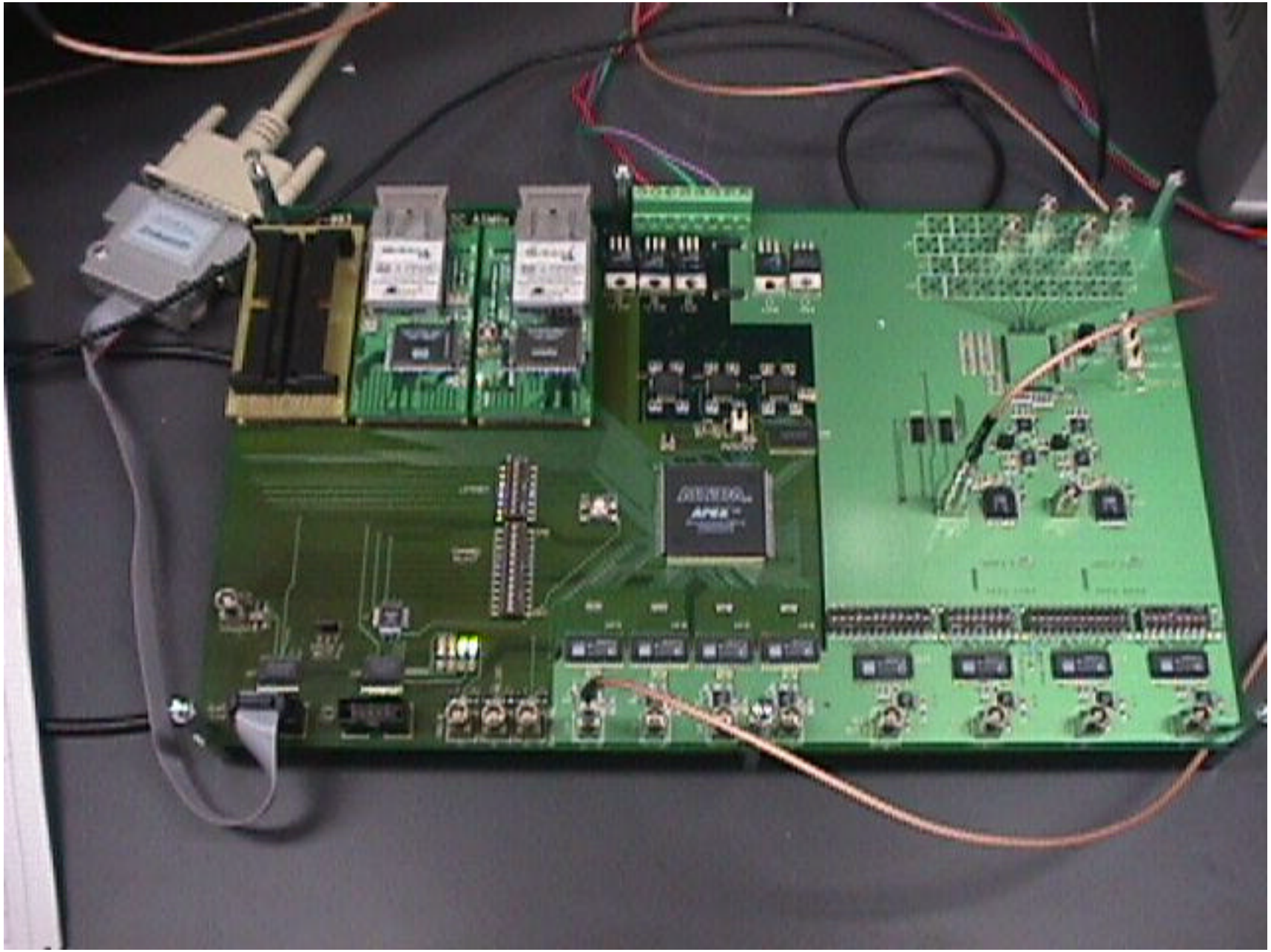


ASMIIa Block Diagram



24 - Channel
ASM II PROTOTYPE BOARD
Kurt Vetter

ASMIIa Prototype



DESIGN DETAILS

Power, Ground and Cooling

- 73W max per faraday shield (2-ASMII's, 4-ASMI's)
- ASMII requires +5v (5.5 amps max)
- ASMI requires +3.3v (1.36 amps max)
- Ground from ASMII to Faraday shield through ASMI?
- Cooling pipe circulates through faraday shield
- Thermal padding between ASMII and faraday shield
- Faraday shield bolted to chamber
- Bolt's pick up ASM ground planes

	1- GLink Tx (HDMP1022) 1- GLink Rx (HDPM1024)	2-Glink Tx's 1-Glink Rx
ASM I	4.5 watts per ASMI (47mw per channel)	4.5 watts per ASMI (47mw per channel)
ASM II	25.2 watts (5.04amps@5V) per ASMII	27.5 watts (5.5amps@5V) per ASMII
Total per half chamber, (inside 1-Faraday shield)	68.4 watts	73 watts

Analog Design

CHALLANGES

- Pre-Amp to SCA interface
- SCA readout = 6.67MHz
- ADC performance
- Board Layout and cooling

Main Components

- **SCA**
  - 144x16 cells
  - 40MHz sampling rate
  - 8MHz readout?
  - 5V supply (1v-4v input linear dynamic range)

- **AD9042 (ADC)**

- 12 bits	- Thermal noise = 0.33LSB	- DNL = +-0.4LSB
- 600mw	- Input BW = 100MHz	- INL = +-0.75LSB
- +5V supply	- Analog in = Vref +-0.5v	- SNR = 67dB

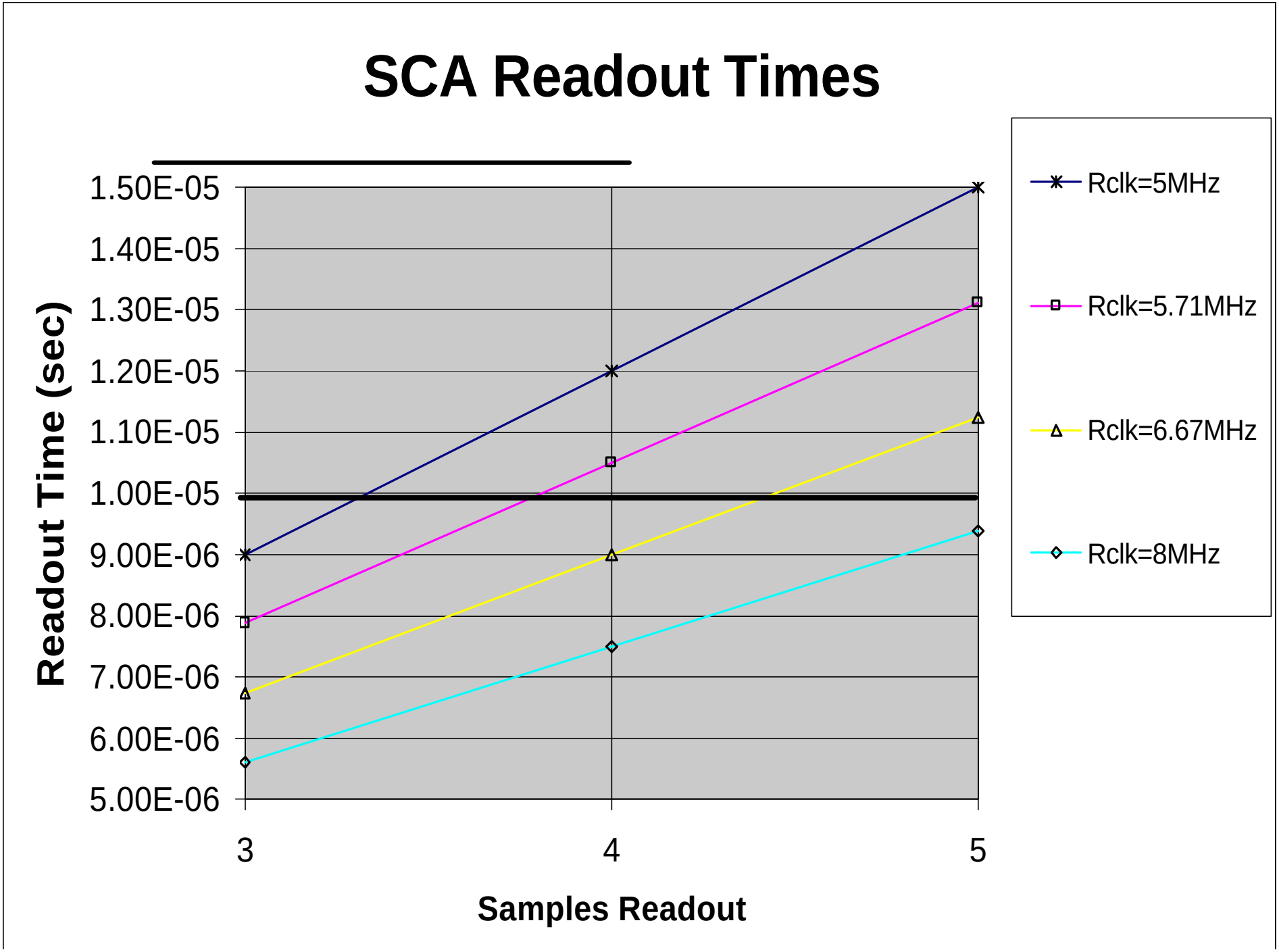
* SNR degredation of 1.4dB due to radiation was observed.

Digital Design

- Readout Requirements
- Readout Constraints
- Readout Numerology
- Readout Architectures

Data Flow Requirements

- Transmit (4x16) 12-bit samples within 10us.
- Transmit on-board current and temperature data as 12-bit words. Data will be fused into main data stream.
- Transmit board identification (board ID).
- Receive and initiate calibration sequence.


SCA Readout Times
Readout Time (sec)
1.50E-05
1.40E-05
1.30E-05
1.20E-05
1.10E-05
1.00E-05
9.00E-06
8.00E-06
7.00E-06
6.00E-06
5.00E-06
3
4
5
Samples Readout
Rclk=5MHz
Rclk=5.71MHz
Rclk=6.67MHz
Rclk=8MHz

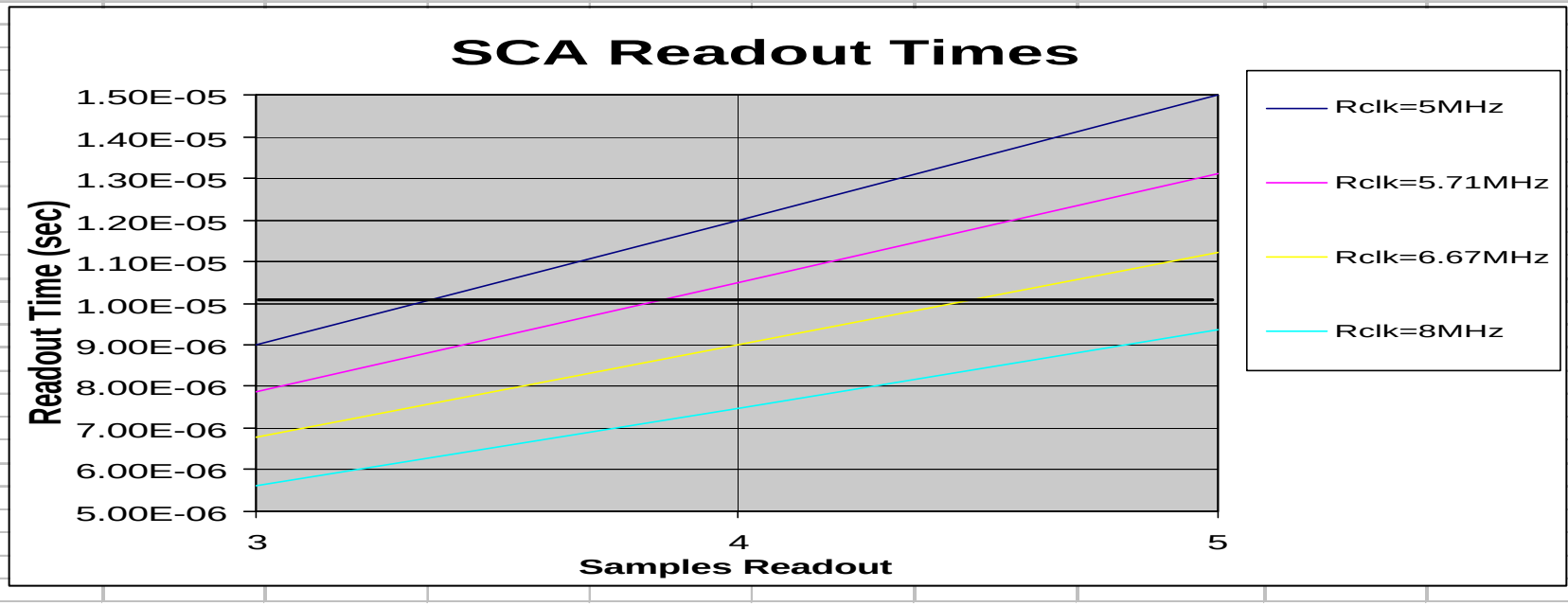
SCA Readout Numerology

ASMII READOUT NUMEROLOGY

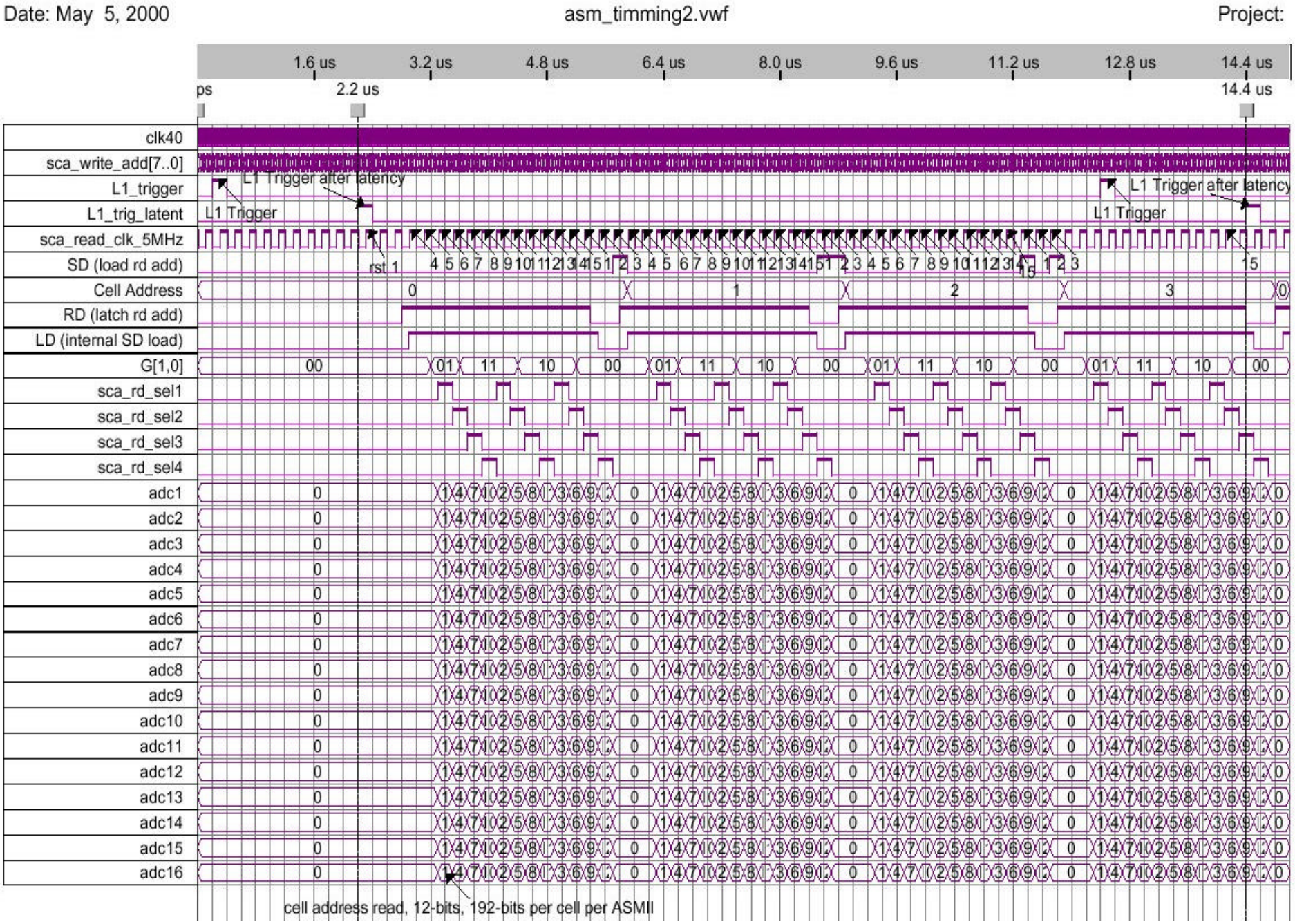
Kurt Vetter
4/25/00

KNOWN PARAMATER DESCRIPTION	**PARAMATER**			
Trigger Rate = 100KHz	1.00E+05			
Readout time (1/Trigger Rate)	1.00E-05			
N = samples	3	4	5	
bits per ADC conversion	10	12		
192 channels per ASMII	192			
16 SCA's per ASMII	16			
Write Clock = 40MHz	4.00E+07			
Clock Divisor = k	8	7	6	5
Read Clock = 40MHz/k	5.00E+06	5.71E+06	6.67E+06	8.00E+06
SCA per sample readout time (15 read clocks for 12-channels)	3.00E-06	2.63E-06	2.25E-06	1.88E-06

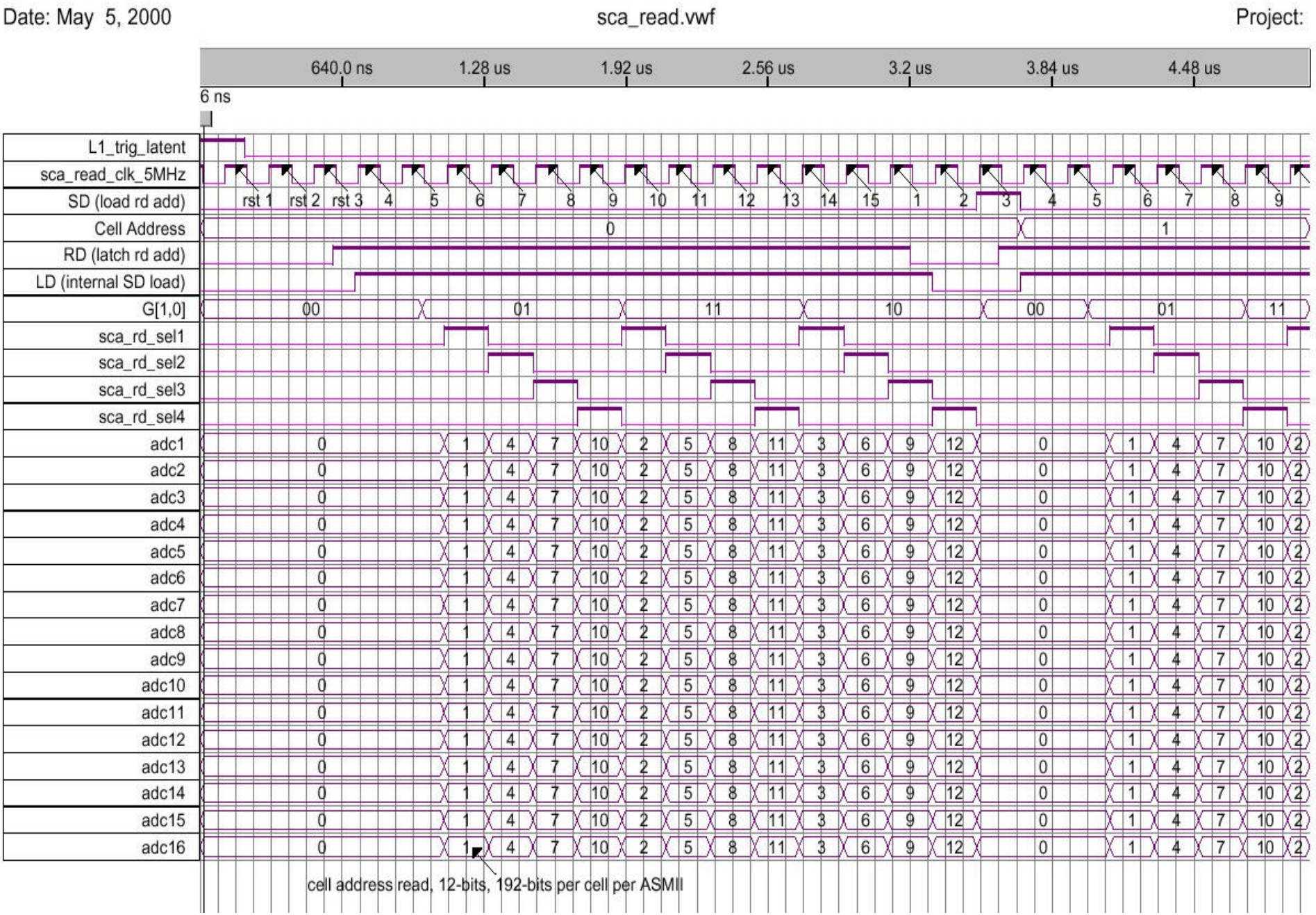
Readout Clock	**Number of samples**	**SCA Readout Time**
5MHz	3	9.00E-06
	4	1.20E-05
	5	1.50E-05
5.71MHz	**3**	**7.88E-06**
	4	**1.05E-05**
	5	**1.31E-05**
6.67MHz	3	6.75E-06
	4	9.00E-06
	5	1.13E-05
8MHz	**3**	**5.63E-06**
	4	**7.50E-06**
	5	**9.38E-06**



Four Sample(12 ch. Per sample) SCA readout



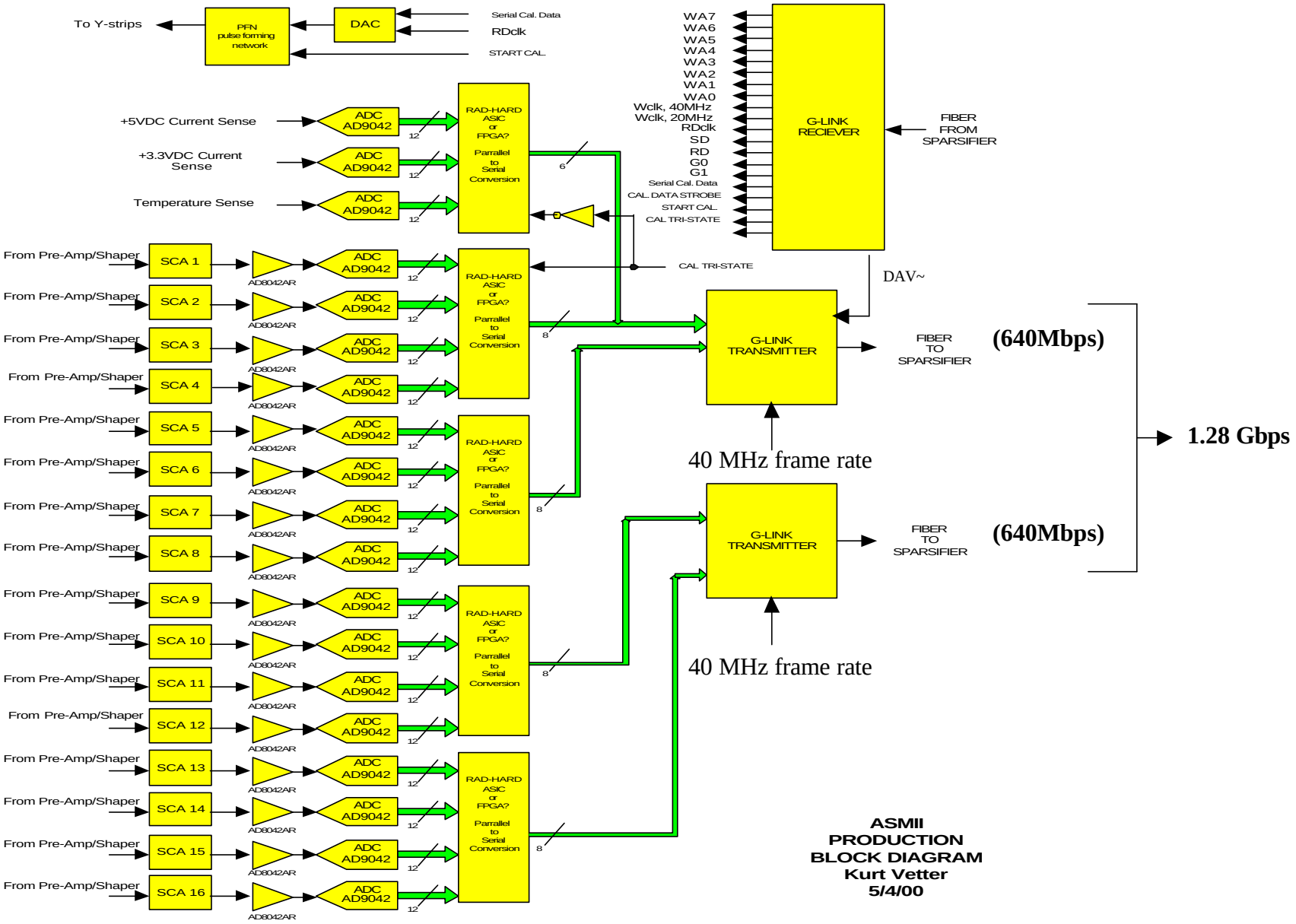
Single Sample (12 channel) SCA readout



ADC Readout Architectures

- Requires only shift-register functionality.
- Possible approaches
  - Custom ASIC (expensive)
  - Off the shelf shift registers (cheap, subject to SEU, so what? This only means a single bit of one sample will be in error)
- May need to implement control logic on ASMII for calibration and monitoring?
- Following diagram illustrates technology independent implementation.

ASMII Readout Scheme Block Diagram



Possible Optical Link Configurations

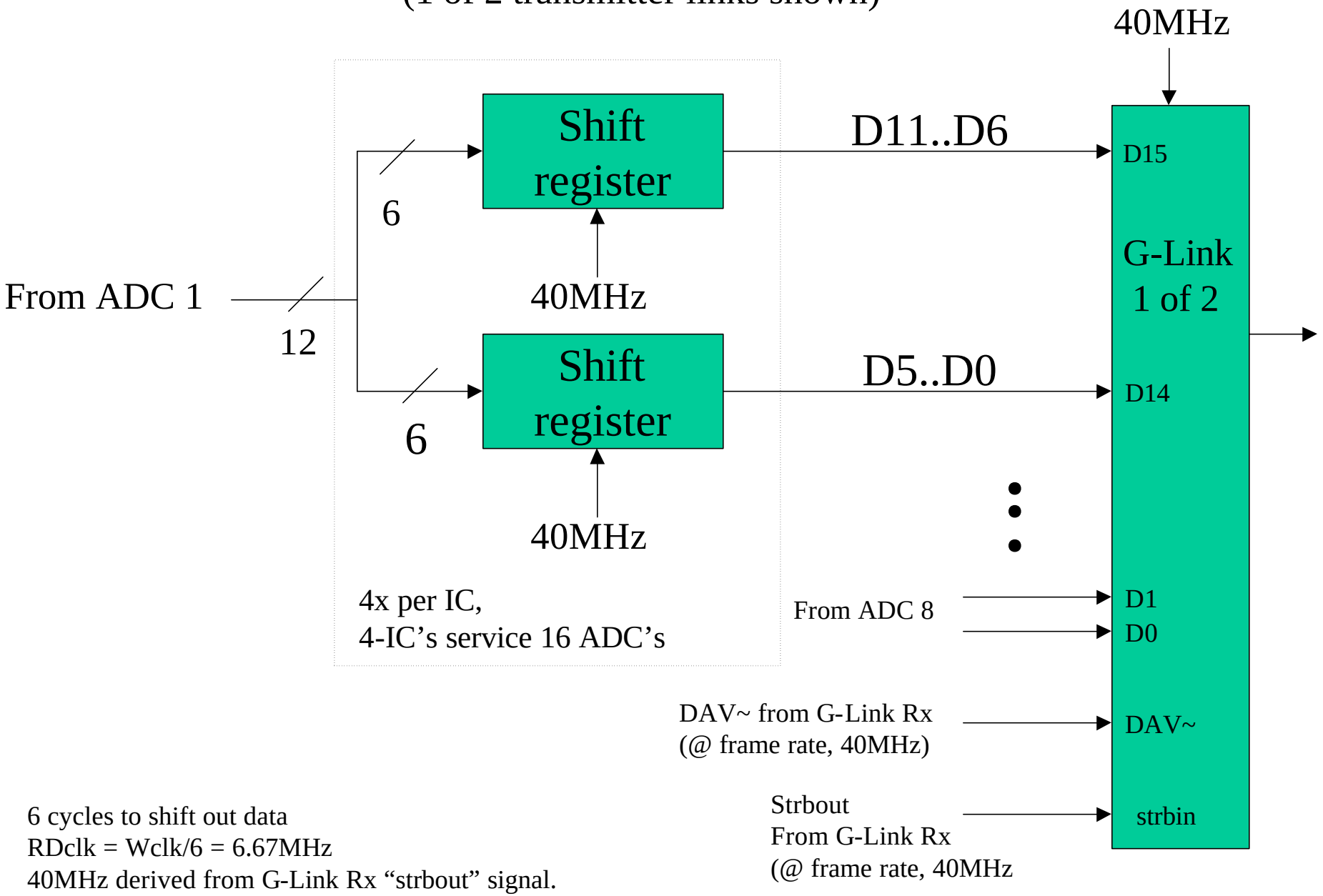
(Consider only G-Link at this time)

LINK CONFIGURATION	COMMENTS
Two Links @ 40MHz (SFM) 2-bits per ADC	Cannot support 5-samples. 4-samples may be tight.
Single Link, double frame Mode 2-bits per ADC	Cannot support SCA readout >5MHz.
Two Links double frame mode 4-bits per ADC	Can support 5-samples.

- Double frame mode implies 80MHz frame clock.
- SFM – single frame mode.

Readout Implementation

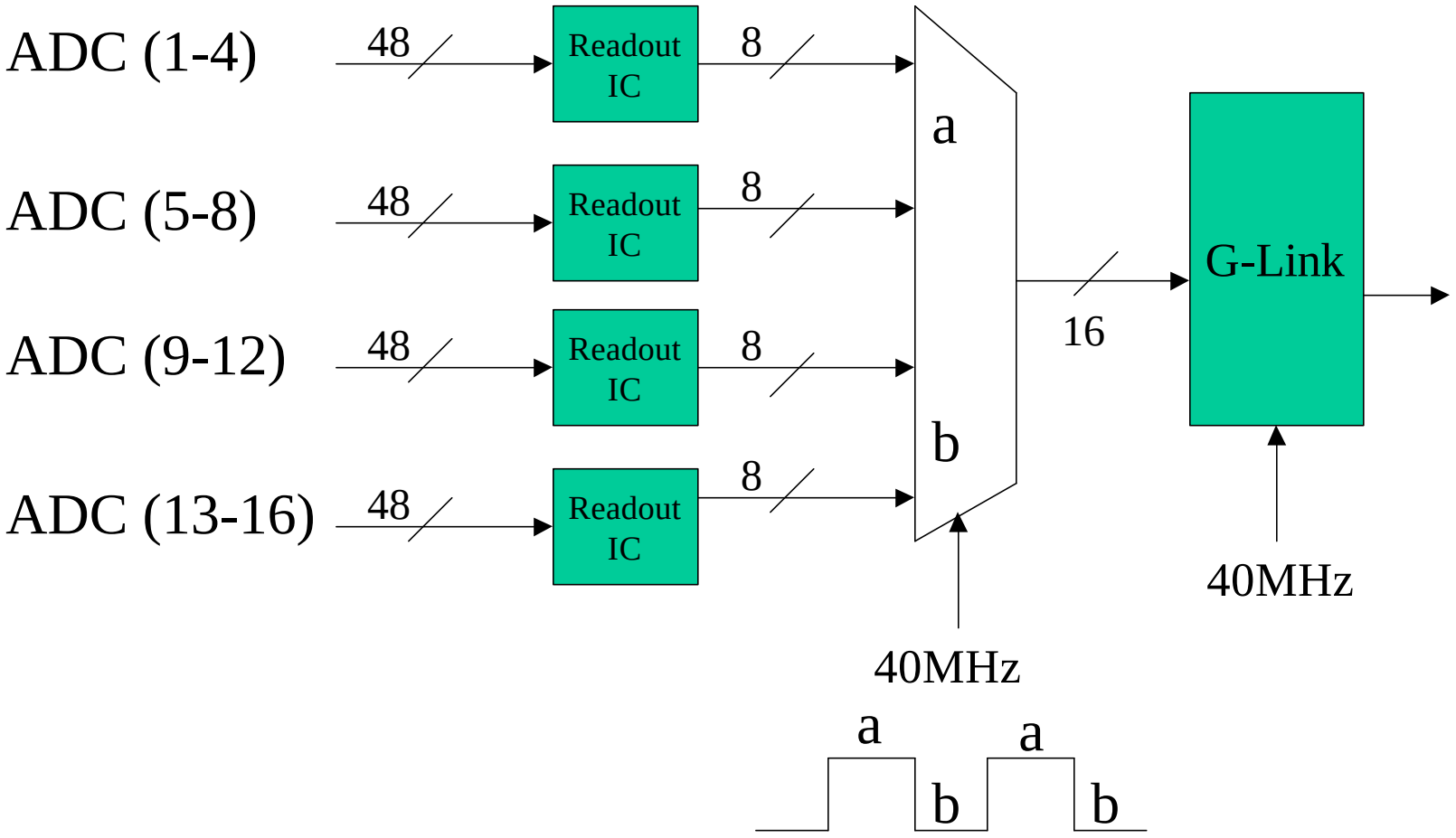
2-Bits per ADC, Single Frame Mode
(1 of 2 transmitter links shown)



6 cycles to shift out data
RDclk = Wclk/6 = 6.67MHz
40MHz derived from G-Link Rx "strbout" signal.
Pipeline cannot accommodate higher readout rates.

Readout Implementation

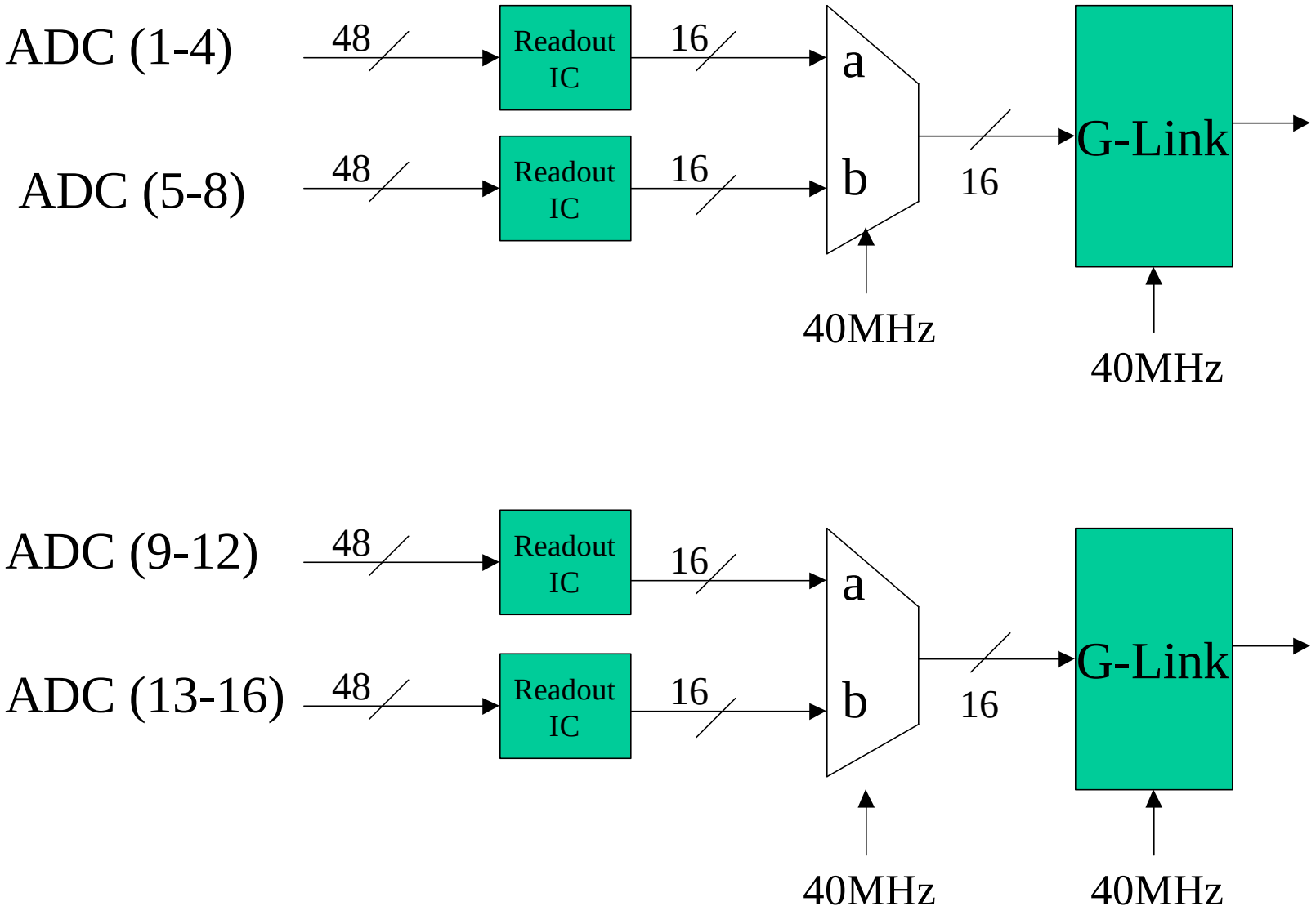
2-Bits per ADC, Double Frame Mode
One Link Required



Can add register before mux at 40MHz.
Select mux at 80MHZ.
80MHz derived from G-Link STRBOUT.

Readout Implementation

4-Bits per ADC, Double Frame Mode



Readout Link Summary

- Serialize ADC's to dedicated G-Link lines
  (2-link lines per ADC)
- SCA readout rate determined by number of time samples.
- Monitored data (supply current, temp)
  fused into one Link.

Optical Links

- One receiver required

- One or two transmitters?
  - Probably two
  - Two links provide inherent redundancy
  - Also more power and space
  - Can run at 40MHz instead of 80MHz

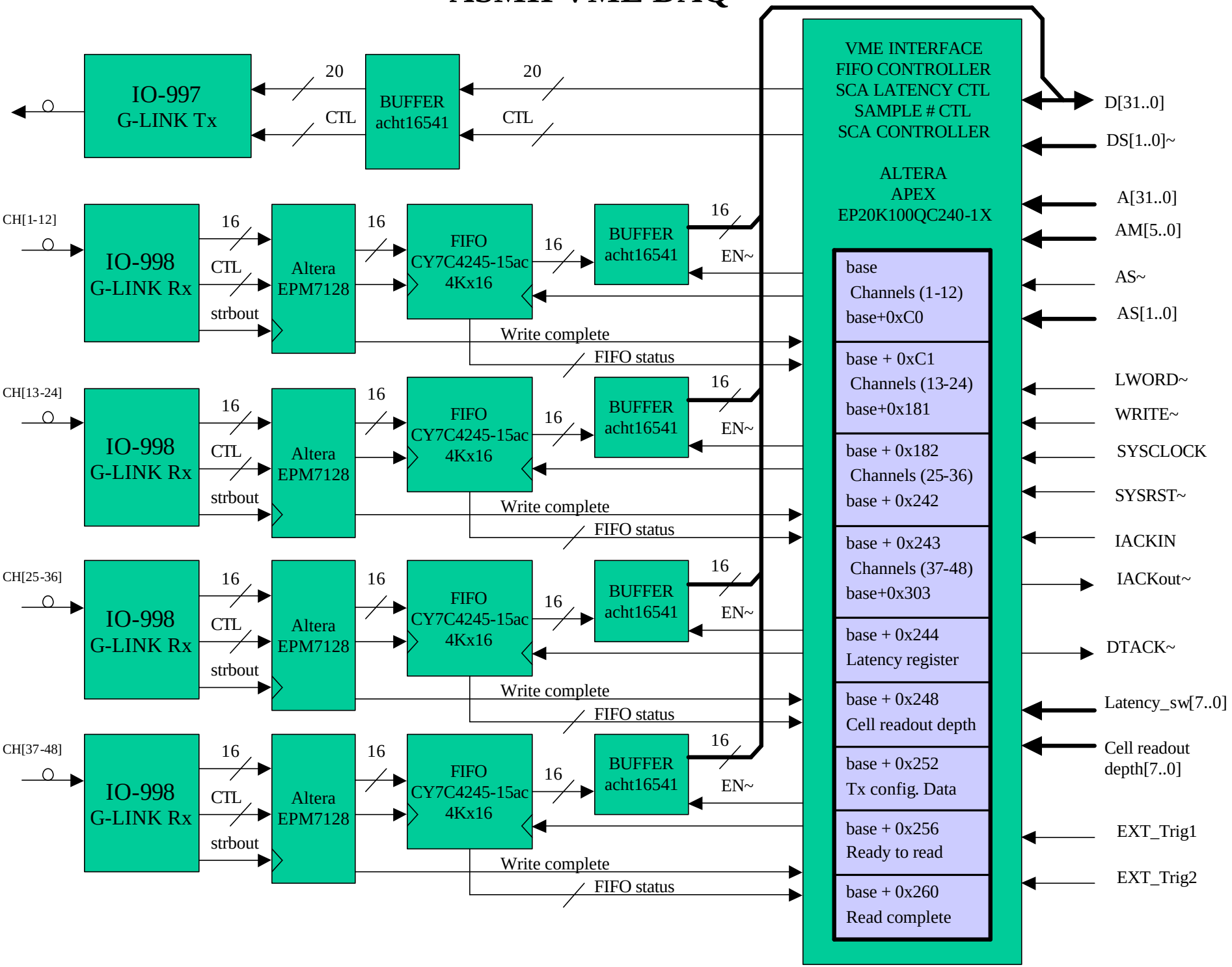
- HDMP 1032/34 available
  - Lower power (590mw Tx, 660mW Rx)
  - Lower BW (1.12 Gbps)
  - 16 bit interface

Radiation

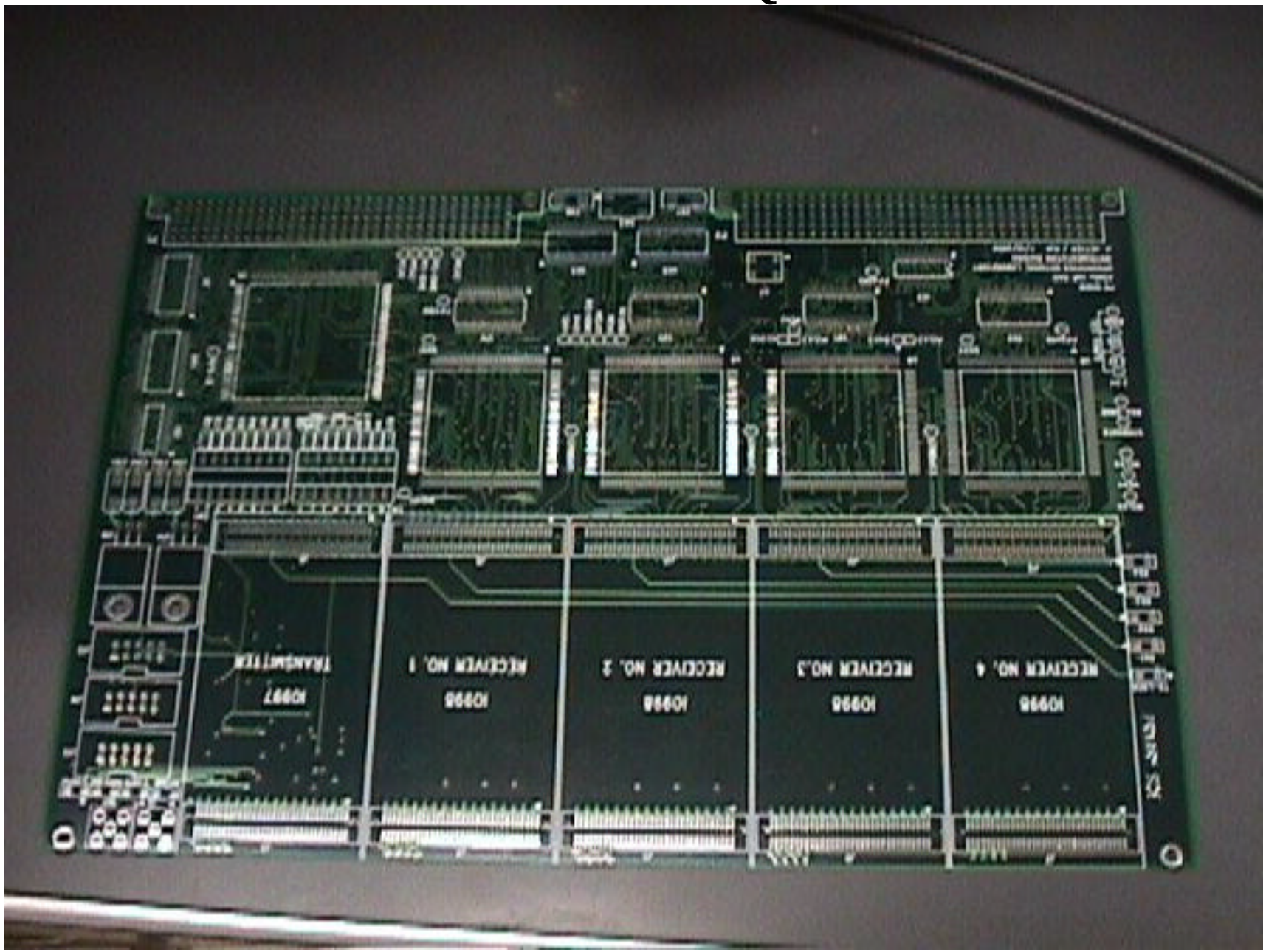
ASMII IC's requiring testing

COMPONENT	COMMENTS
HDMP 1022	Extensive testing has been performed. Plan to conduct our own test.
HDMP 1024	No testing performed. Must test on our own.
SCA	Testing to be completed by LAr.
AD9042 (ADC)	Used on LAr FEB. Extensive testing performed by Denes at Princton.
AD8042 (op-amp)	Used on LAr FEB. Ionizing survival test done by LAr.
Level Translators?	Required for SCA. Need to select and test.
DAC (used for Calibration PFN)	Need to select and test.
Readout Interface IC (FPGA or ASIC?)	Need to choose technology and test.

ASMII VME DAQ



VME DAQ


TRANSMITTER
RECEIVER NO. 1
RECEIVER NO. 2
RECEIVER NO.3
RECEIVER NO. 4